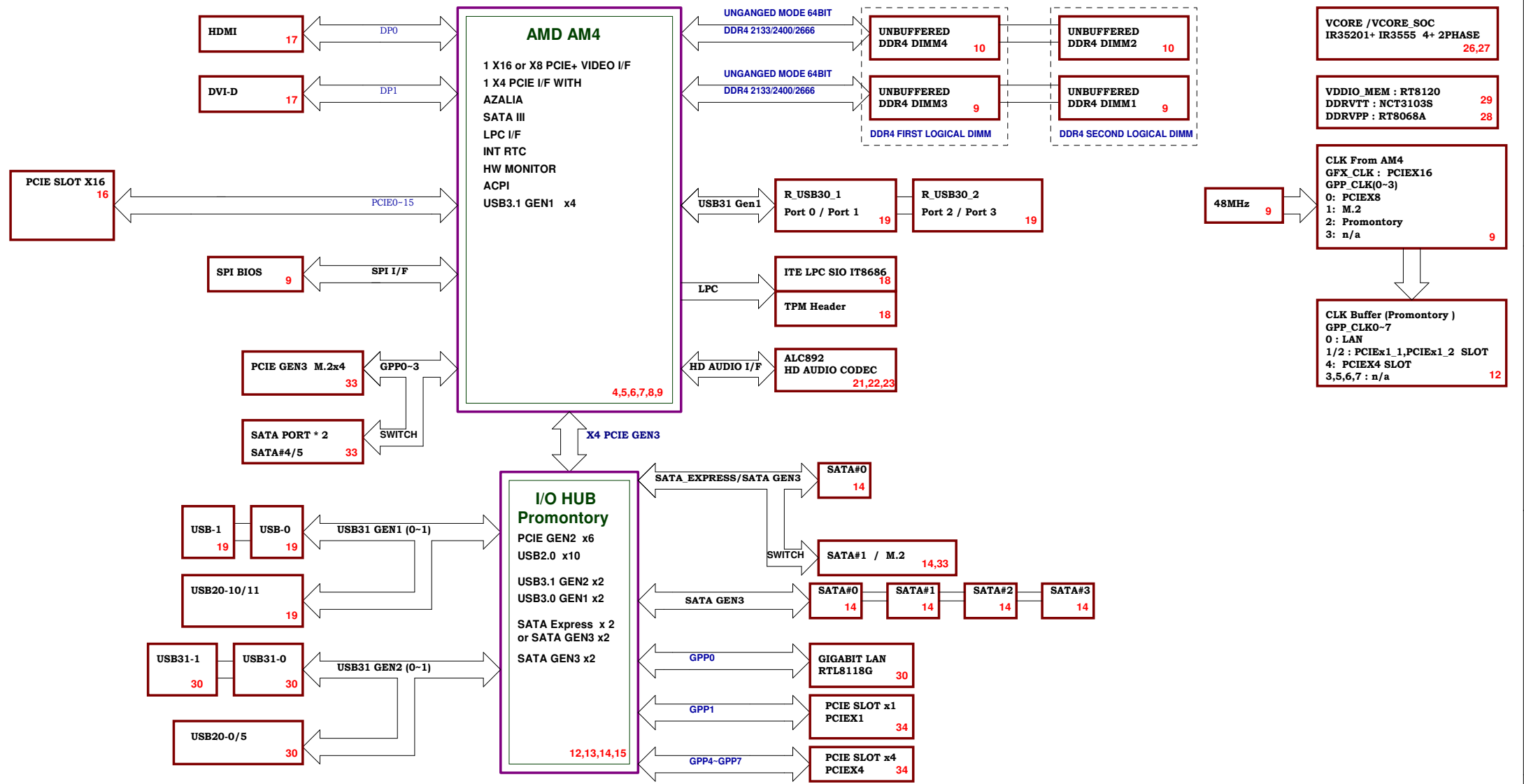


# B450 AORUS M

PAGE	TITLE	Revision : 1.1
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
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12	PM CLK/GPIO/FAN	
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14	PM UMI/GPP/SATA	
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16	PCI EXPRESS x16	
17	HDMI , DVI	
18	IT8686CX , TPM	
19	F_USB30 , R_USB30 , F_USB20	
20	A_VDD1V8 / A_VDDPS5	
21	ALC892 CODEC	
22	AUDIO JACK	
23	AUDIO LED	
24	POWER SEQUENCE , A_VDDP	
25	PWM SL95712	

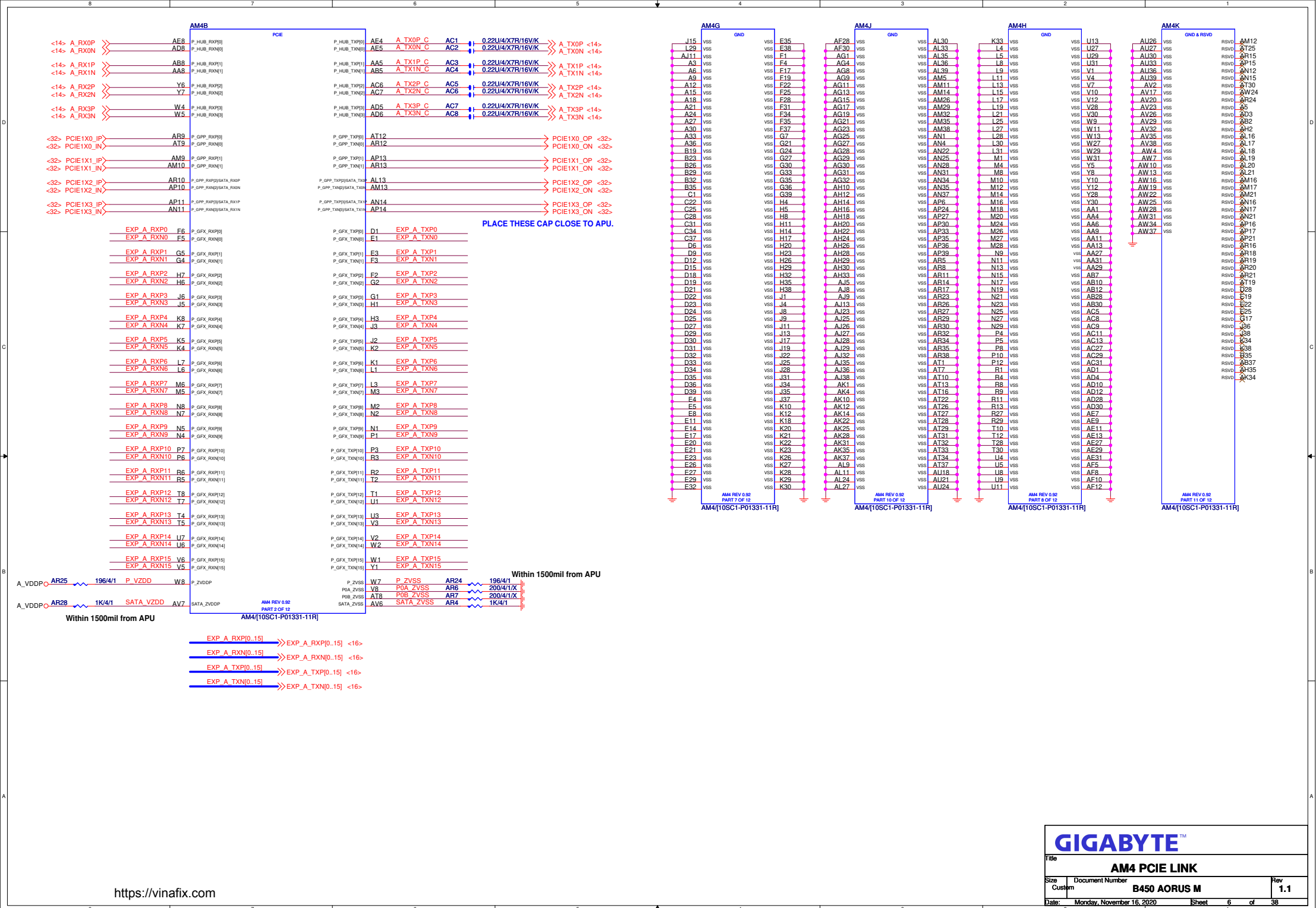
[illegible]

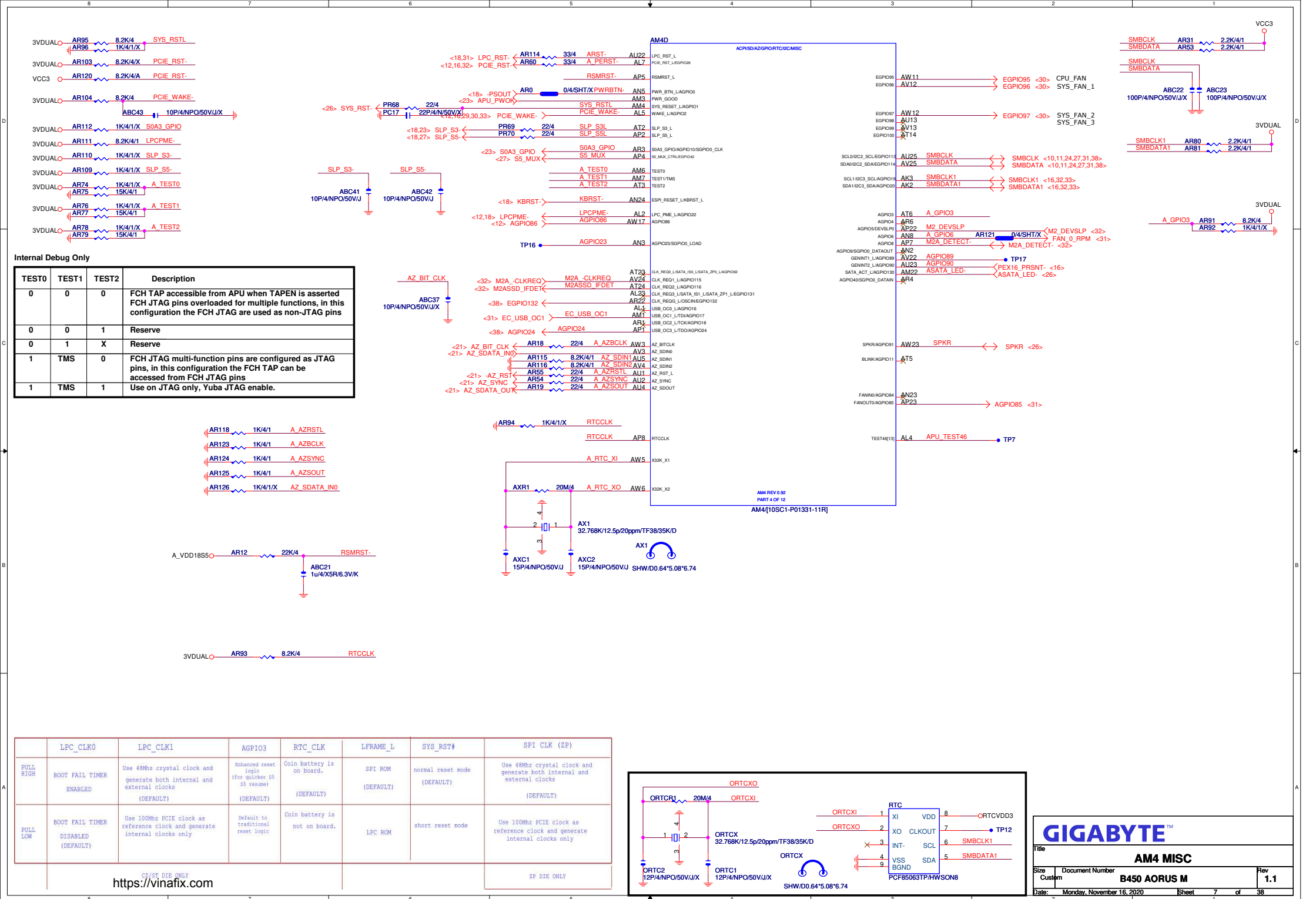


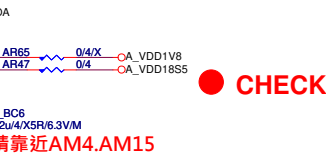
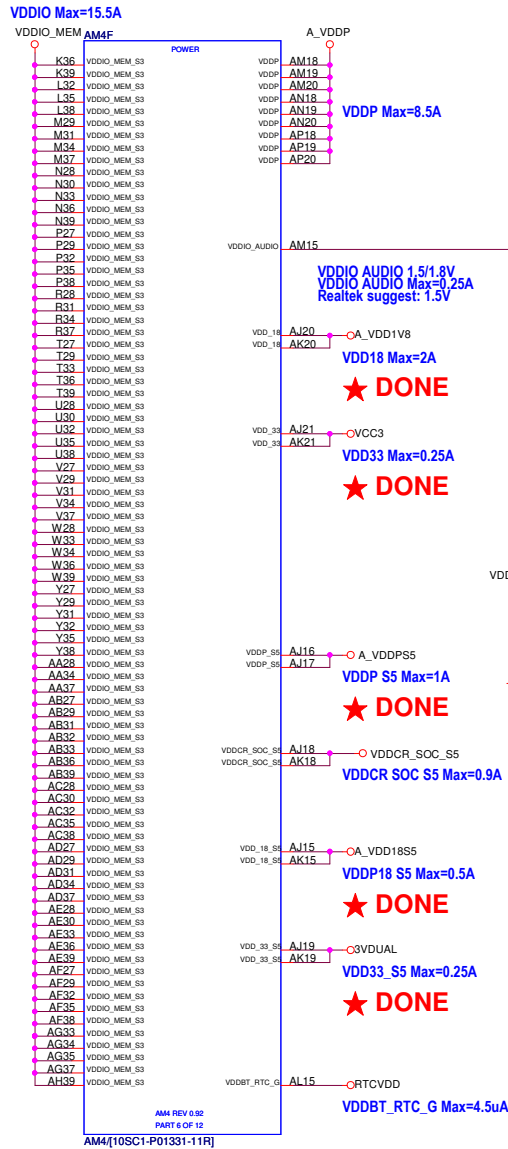




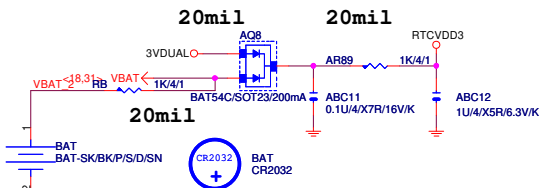
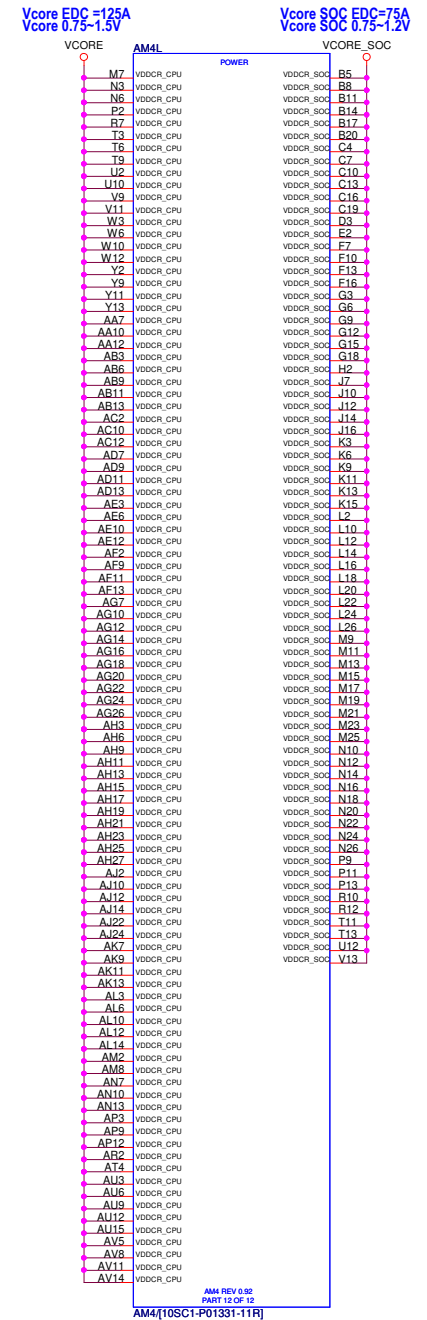
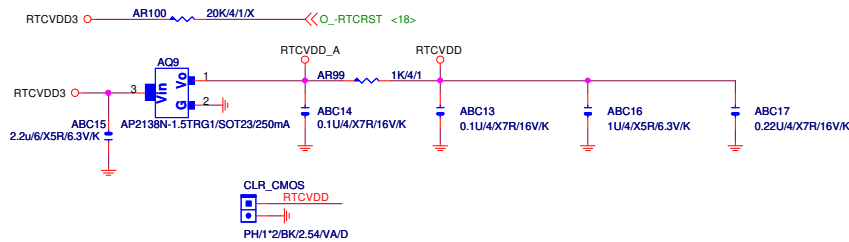
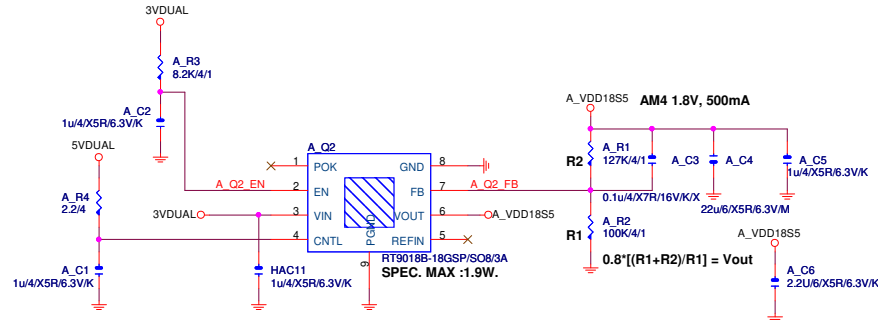
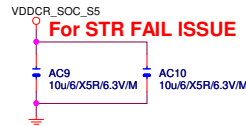








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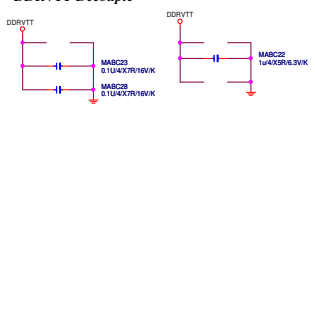
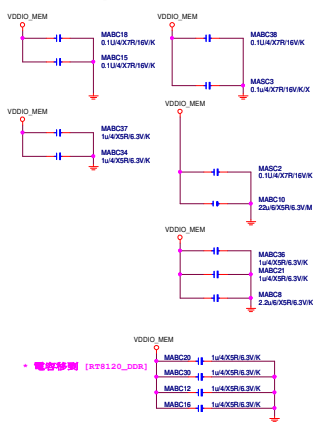
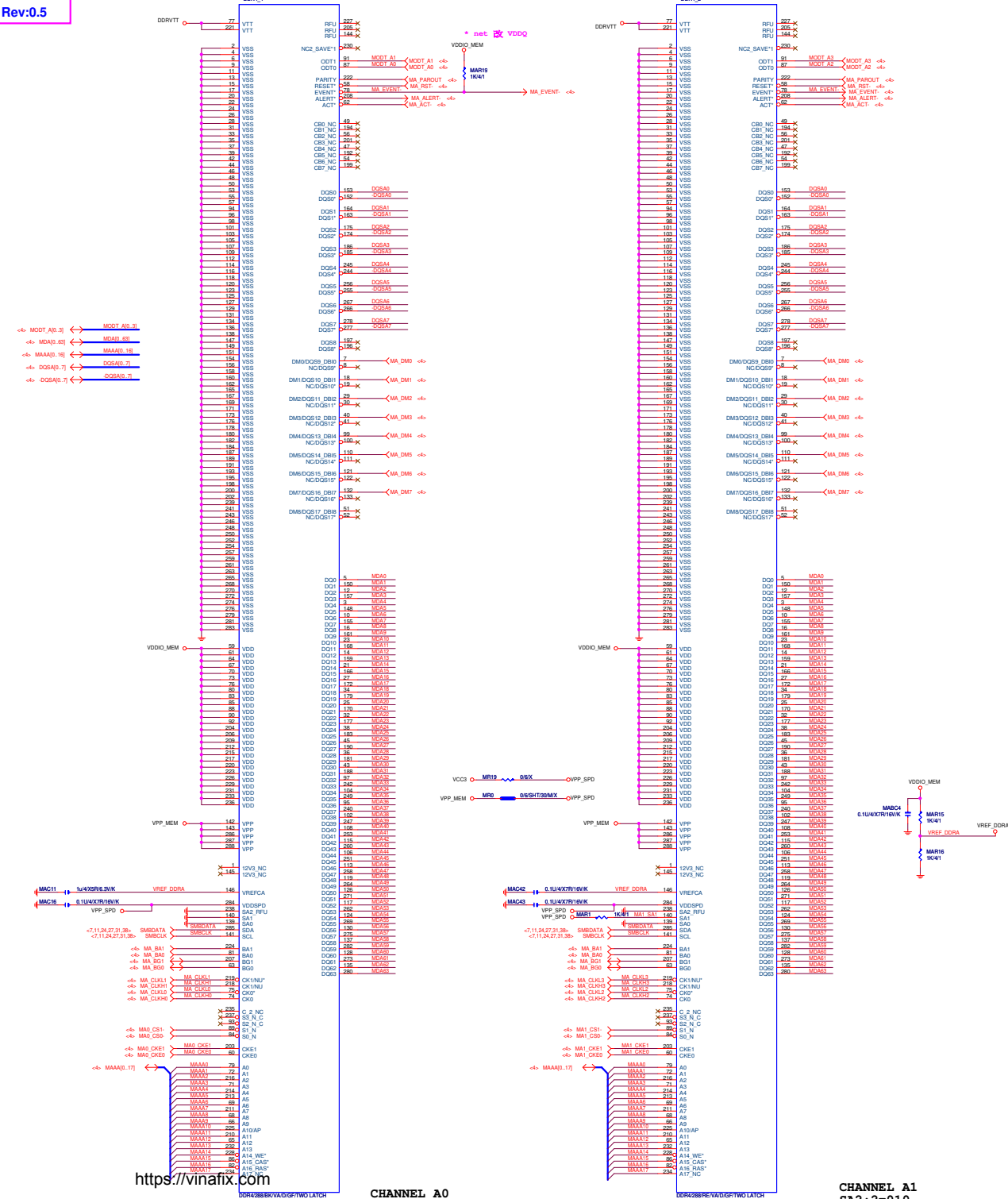
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

GIGABYTE™			
Title CPU POWER & GND			
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Date: Monday, November 16, 2020	Sheet 8	of 38	

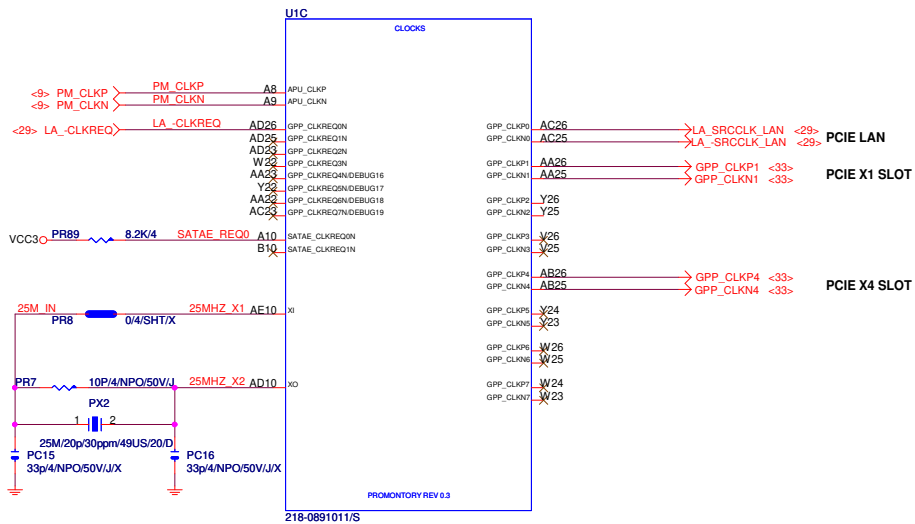
https://vinafix.com



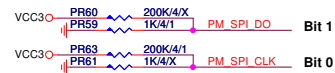




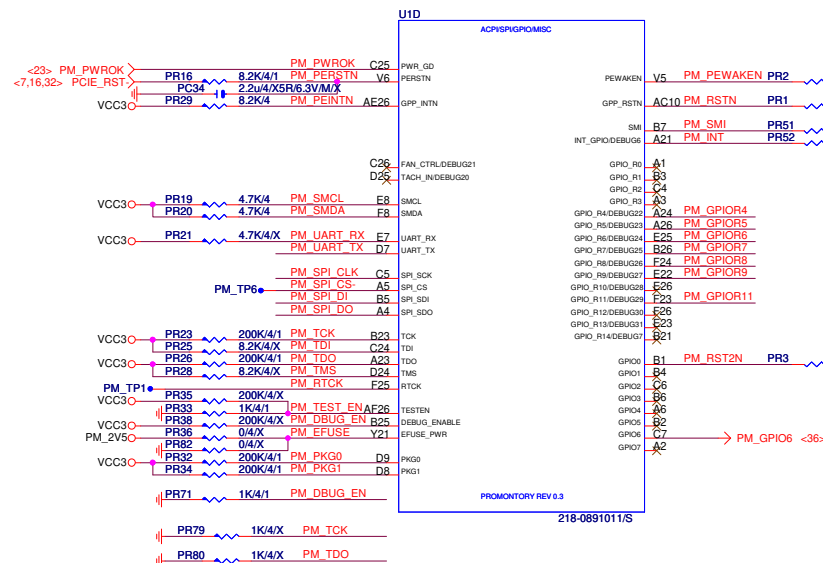




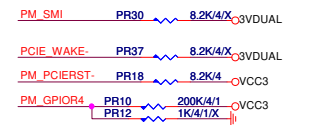
PM GPP Group 0 Strap: 11=> 1PCle x4, 10=>1PCle x2, 2PClex1, 01=>4PCle x1, 00=>Reserved.  
PM GPP Group 0=>0-3



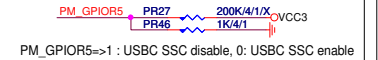
PM GPP Group 1 Strap: 11=> 1PCle x4, 10=>1PCle x2, 2PClex1, 01=>4PCle x1, 00=>Reserved.  
PM GPP Group 1=>4-7



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PM\_GPIOR4 1: GPP clock source from APU\_CLKP/N; 0: GPP clock source from Crystal, also enables GPIO\_R8.



PM\_GPIOR5=>1: USB SSC disable, 0: USB SSC enable



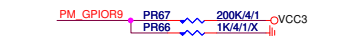
PM\_GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable



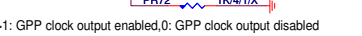
PM\_GPIOR7=>1: SATA Express SSC disable, 0: SATA Express SSC enable



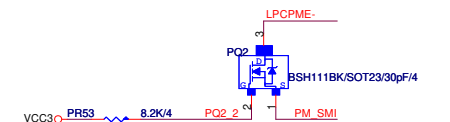
PM\_GPIOR8 (enabled from GPIO\_R4) =>1: GPP SSC disable, 0: GPP SSC enable



PM\_GPIOR9=>1: GPP clock output disabled, 0: GPP clock output disabled



PM\_GPIOR11=>1: GPP clock output disabled, 0: GPP clock output disabled



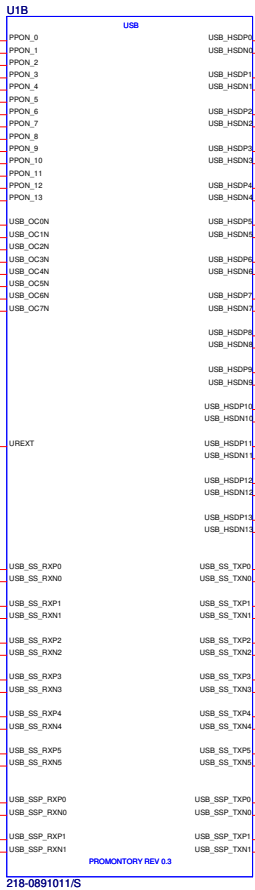
<b>GIGABYTE</b>		ANS 8475214
Title		
<b>B350 CLK GEN / GPIO</b>		
Size	Document Number	Rev
Custom	<b>B450 AORUS M</b>	<b>1.1</b>
Date:	Tuesday, December 15, 2020	Sheet 12 of 38

USB port power control 13:0 (VCC3). Output.

<29> -USBOC\_R1  
<19> -USBOC\_F1

<19> P\_SS\_RX0P  
<19> P\_SS\_RX0N  
<19> P\_SS\_RX1P  
<19> P\_SS\_RX1N

P\_SSP\_RX0P  
P\_SSP\_RX0N  
P\_SSP\_RX1P  
P\_SSP\_RX1N

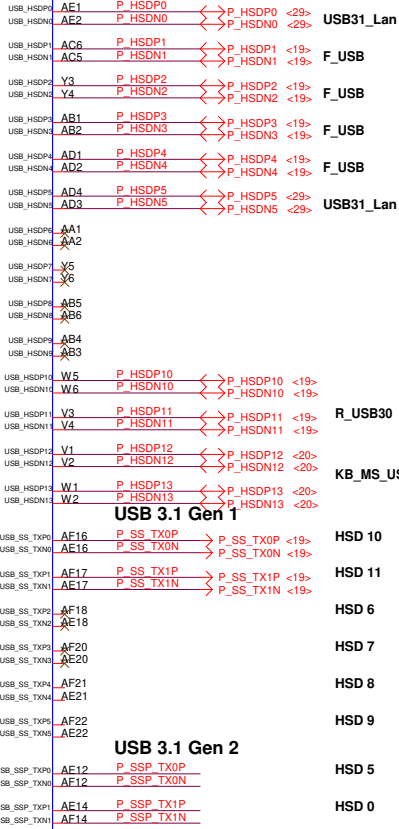


### USB 3.1 Gen 1

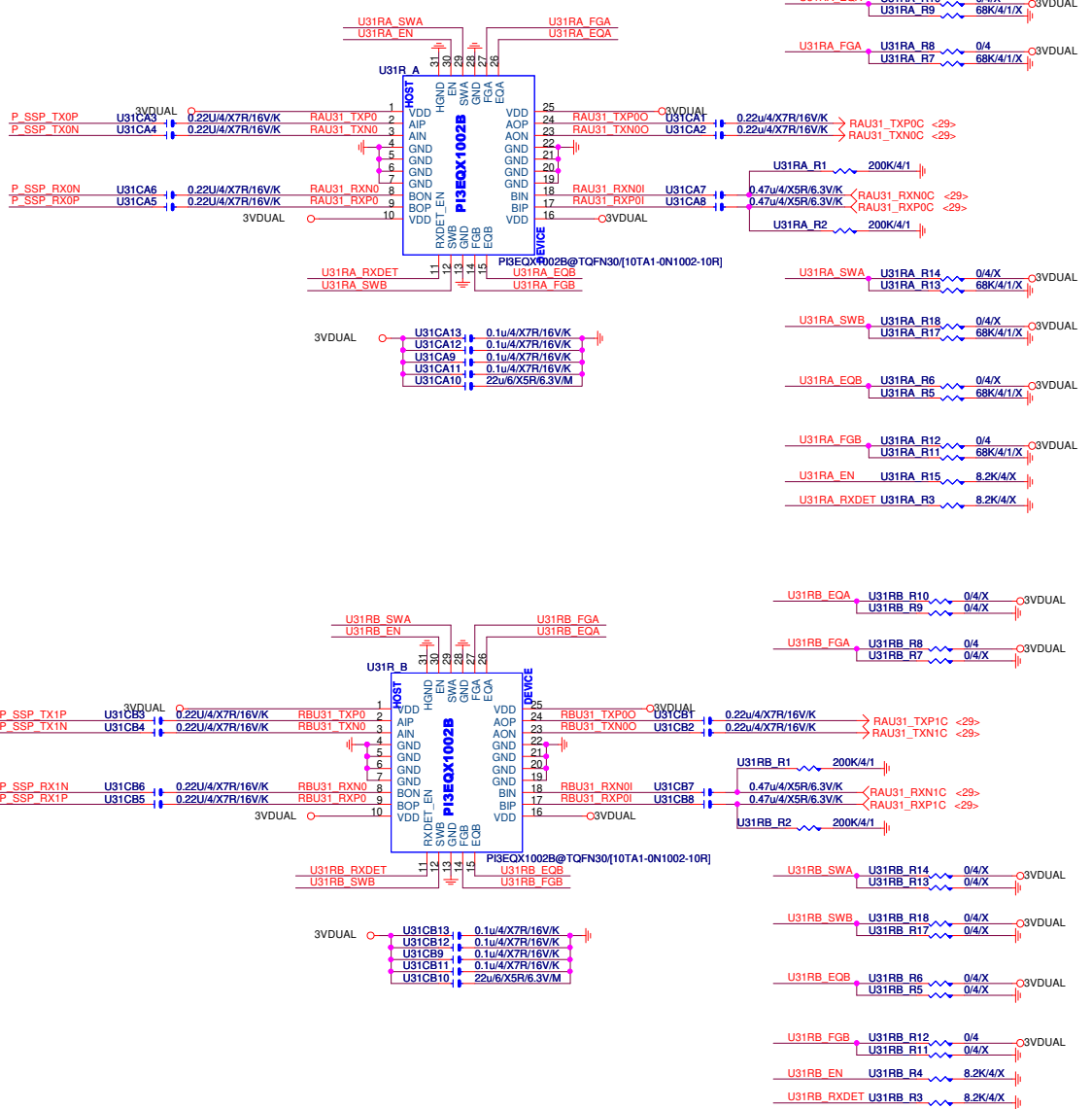
### USB 3.1 Gen 2

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

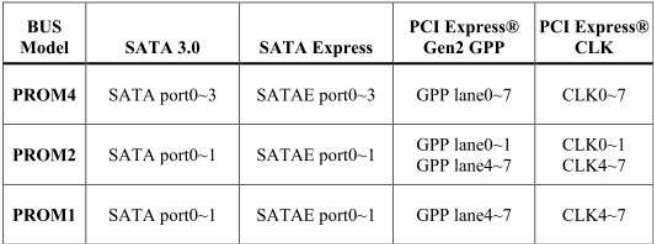
https://vinafix.com

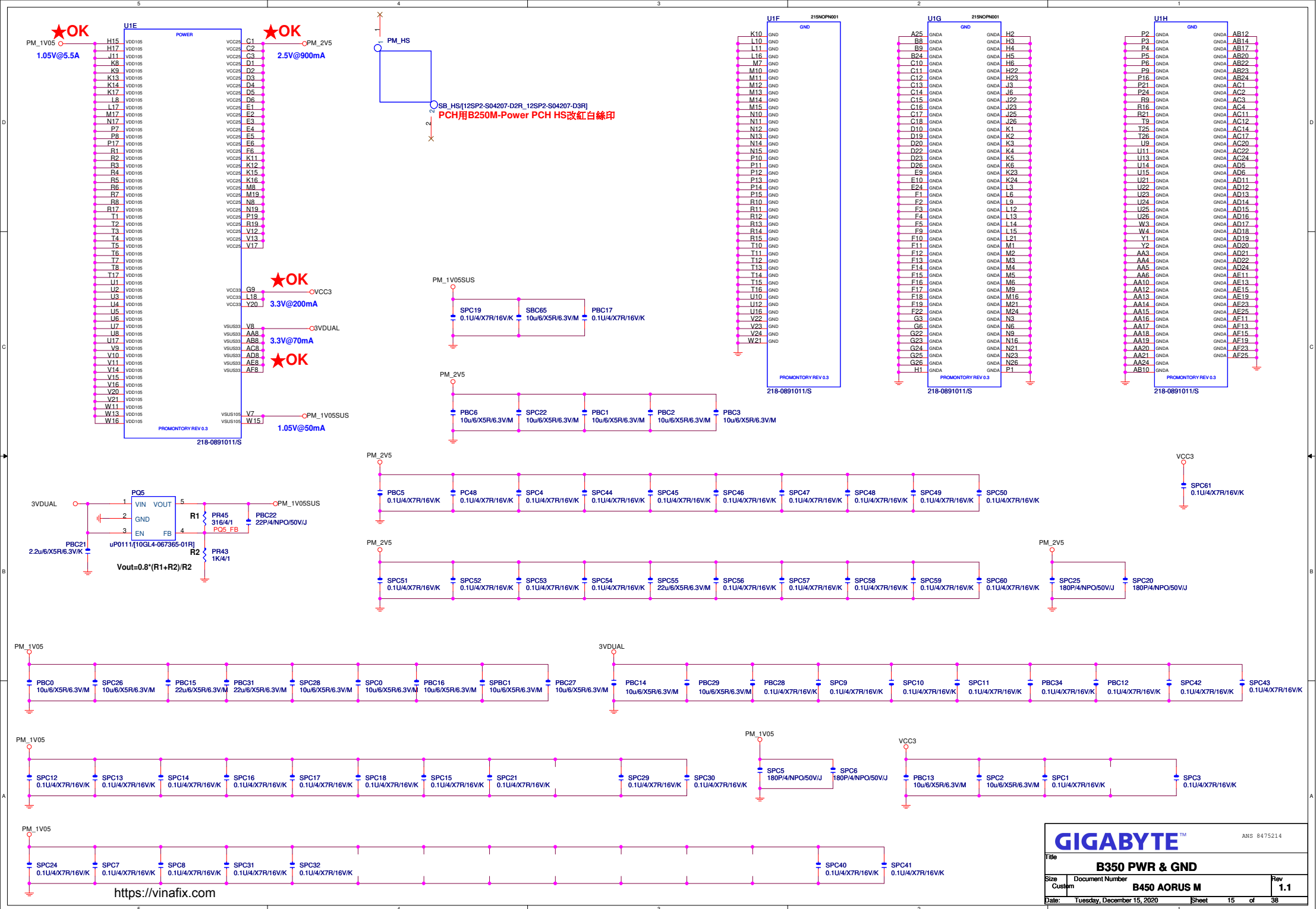


BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

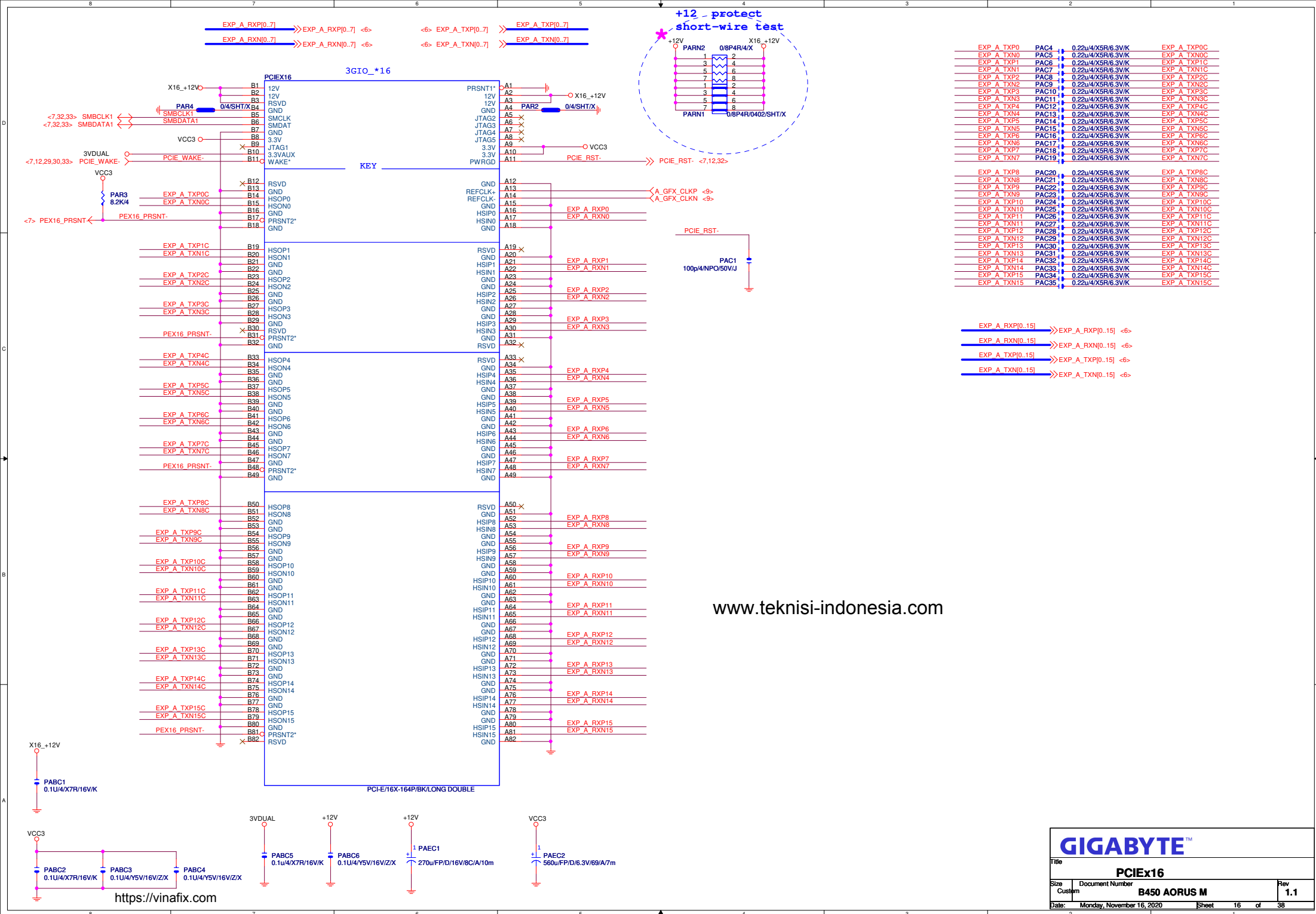


GIGABYTE™				ANS 8475214
Title				B350 USB , PI3EQX1002B
Size				Document Number
Date				B450 AORUS M
Date				Tuesday, December 15, 2020
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Rev				1.1

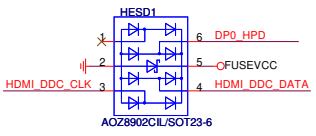
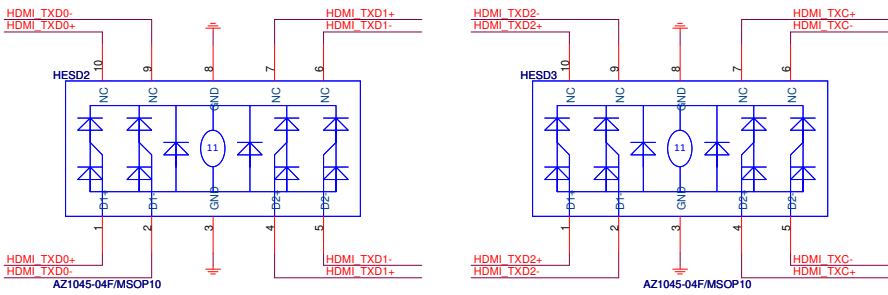
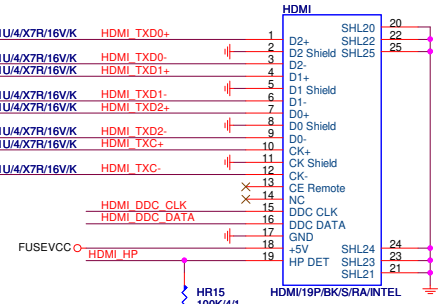
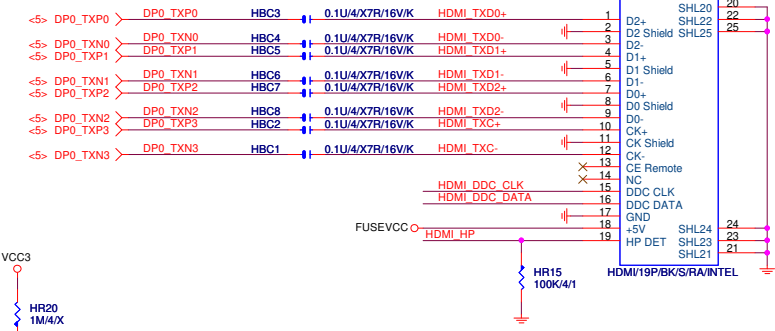
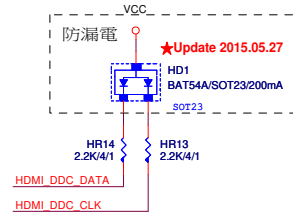
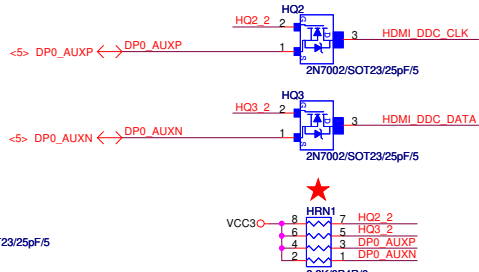
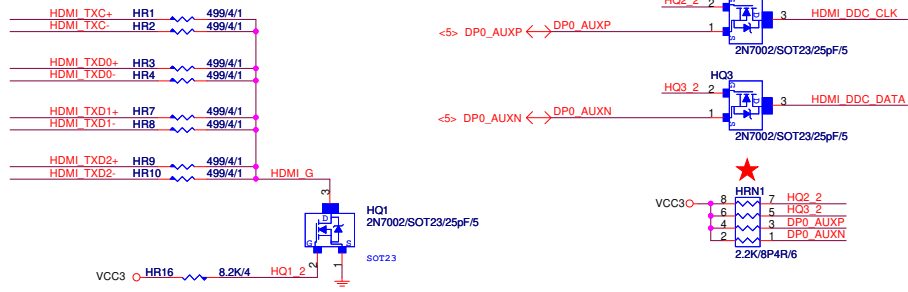








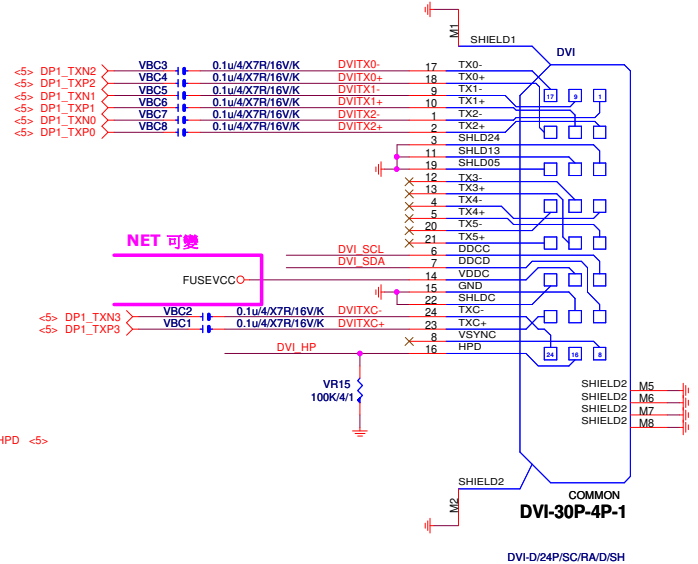
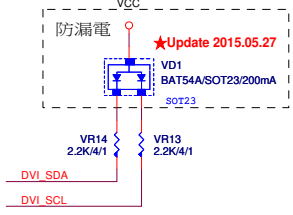
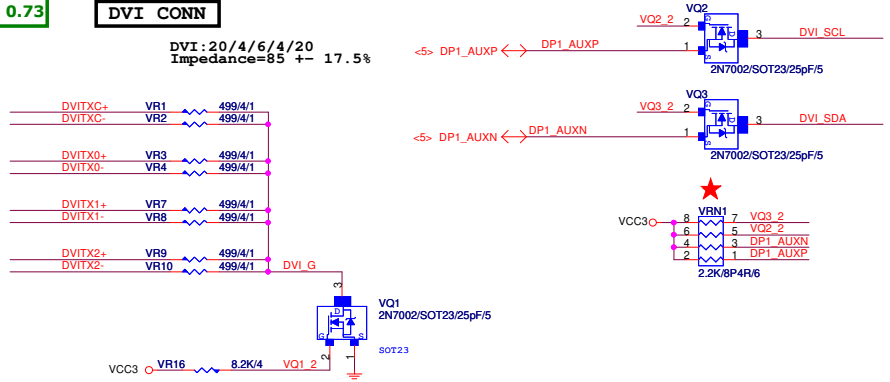




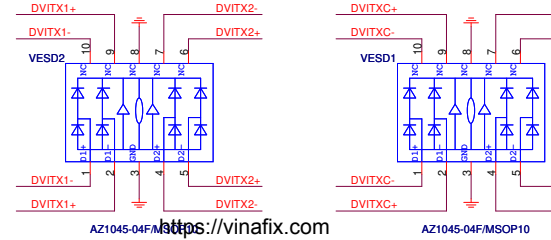
Rev: 0.73

DVI : 20/4/6/4/20  
Impedance=85 +- 17.5%

DVI CONN

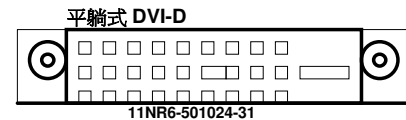


Close to connector



NET 可變

Close to connector



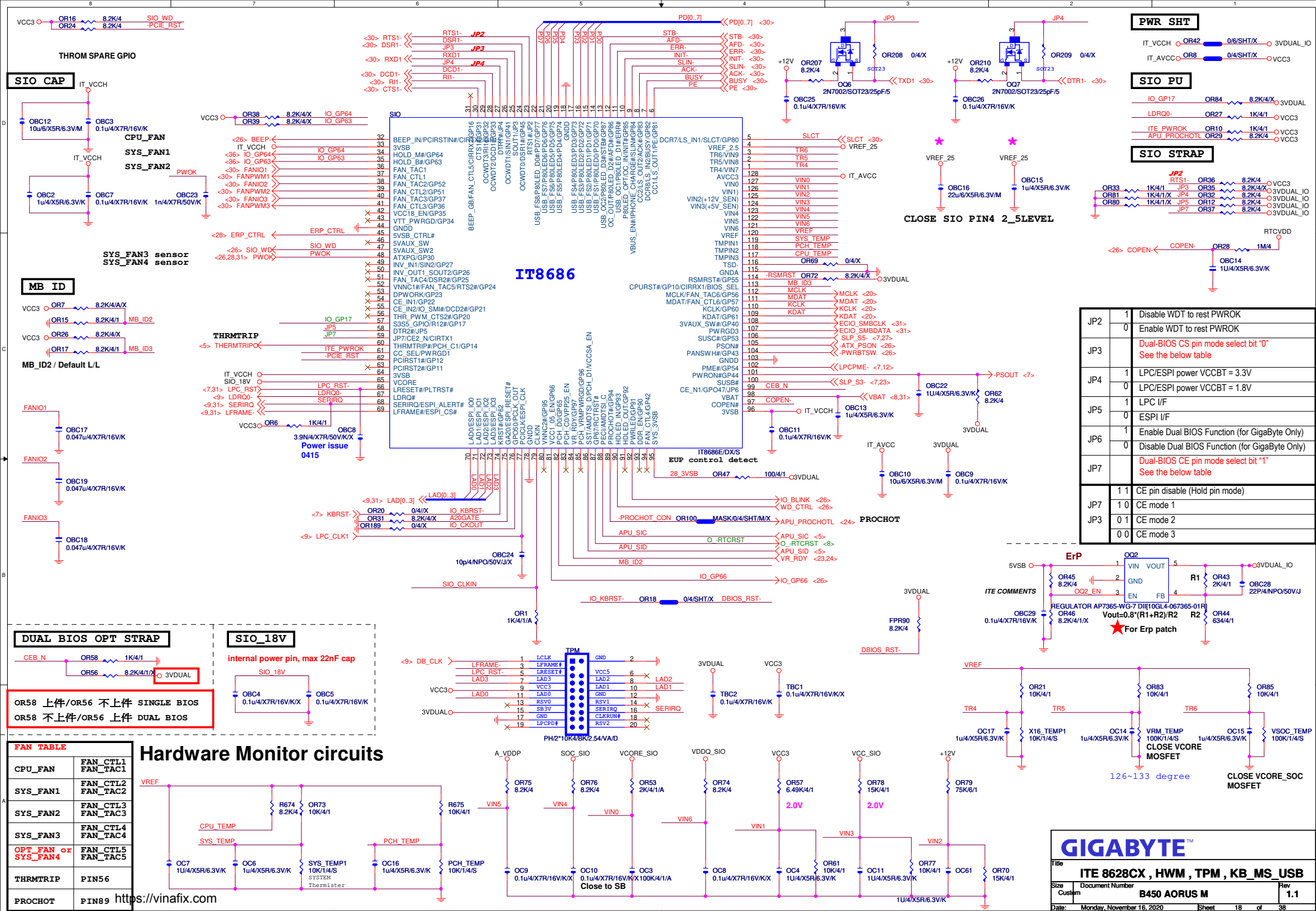
**GIGABYTE**

**HDMI , DVI**

Size: Custom  
Document Number: B450 AORUS M  
Date: Monday, November 16, 2020  
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11NR6-501024-31

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JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual-BIOS CS pin mode select bit "0"
JP3	0	See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7	1	Dual-BIOS CE pin mode select bit "1"
JP7	0	See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3

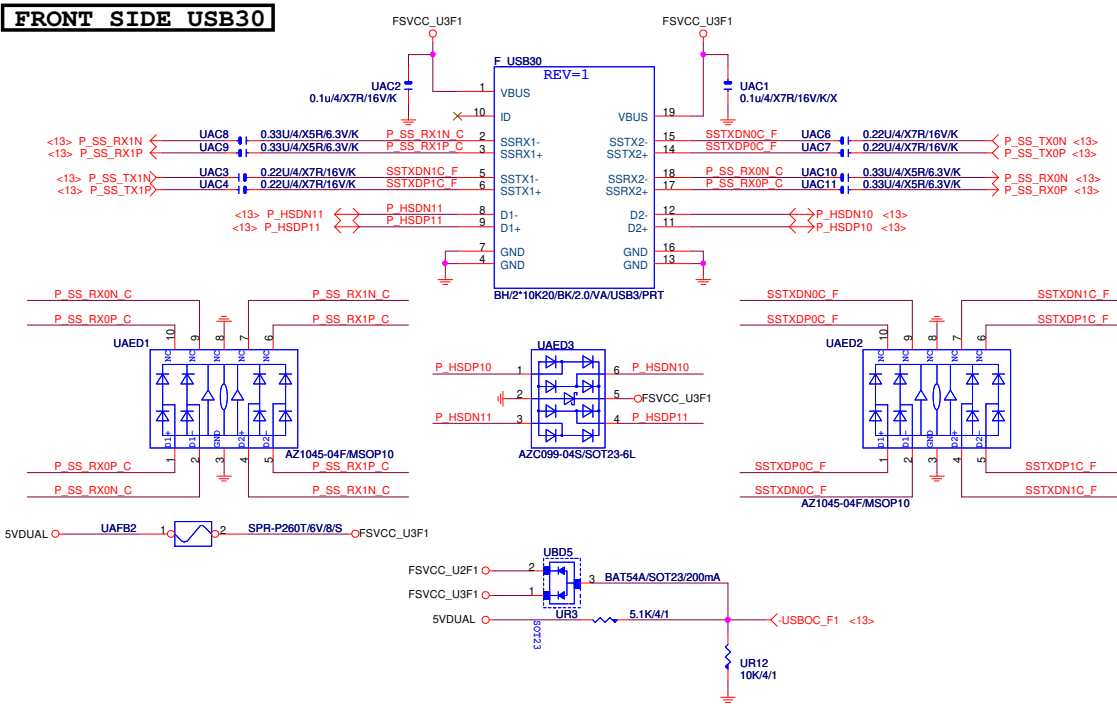
**GIGABYTE**<sup>TM</sup>

**ITE 8628CX , HW M , TPM , KB MS\_USB**

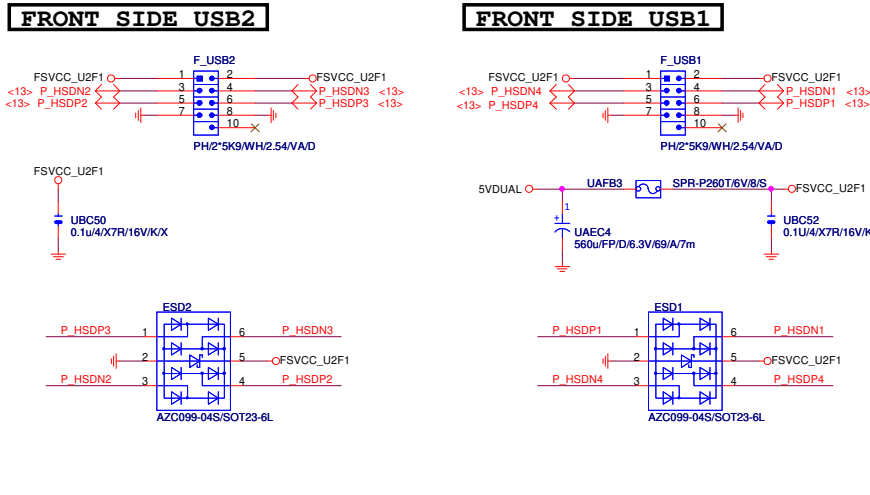
Size: Custom    Document Number: **B450 AORUS M**    Rev: **1.1**

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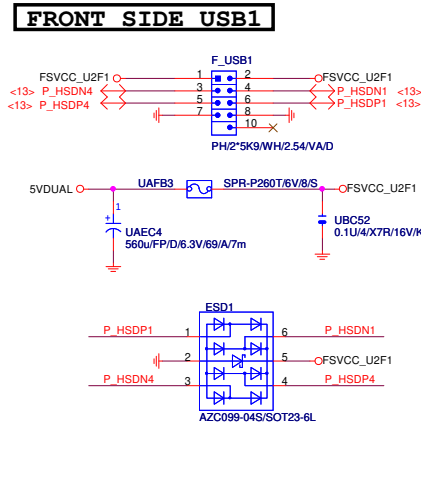
**FRONT SIDE USB30**



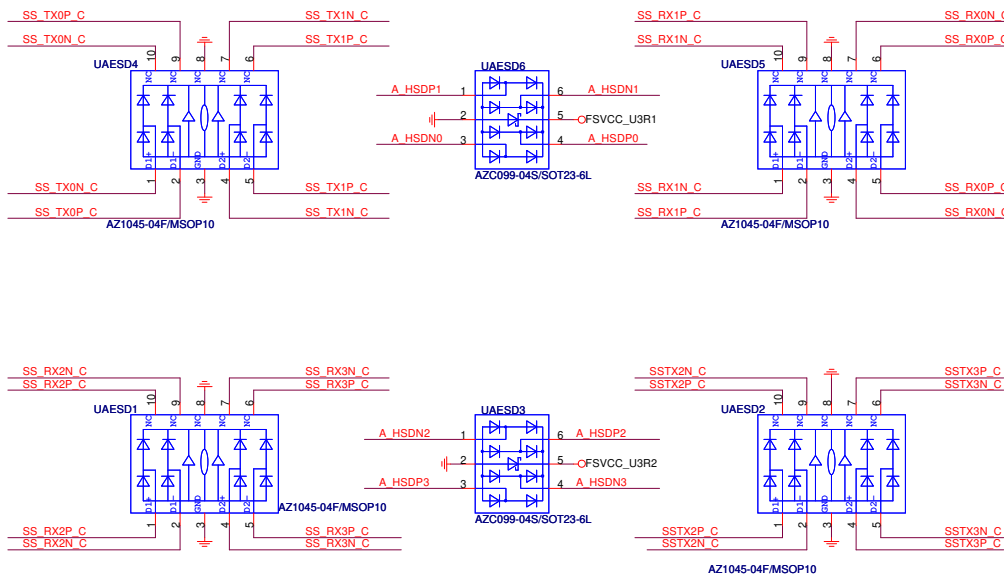
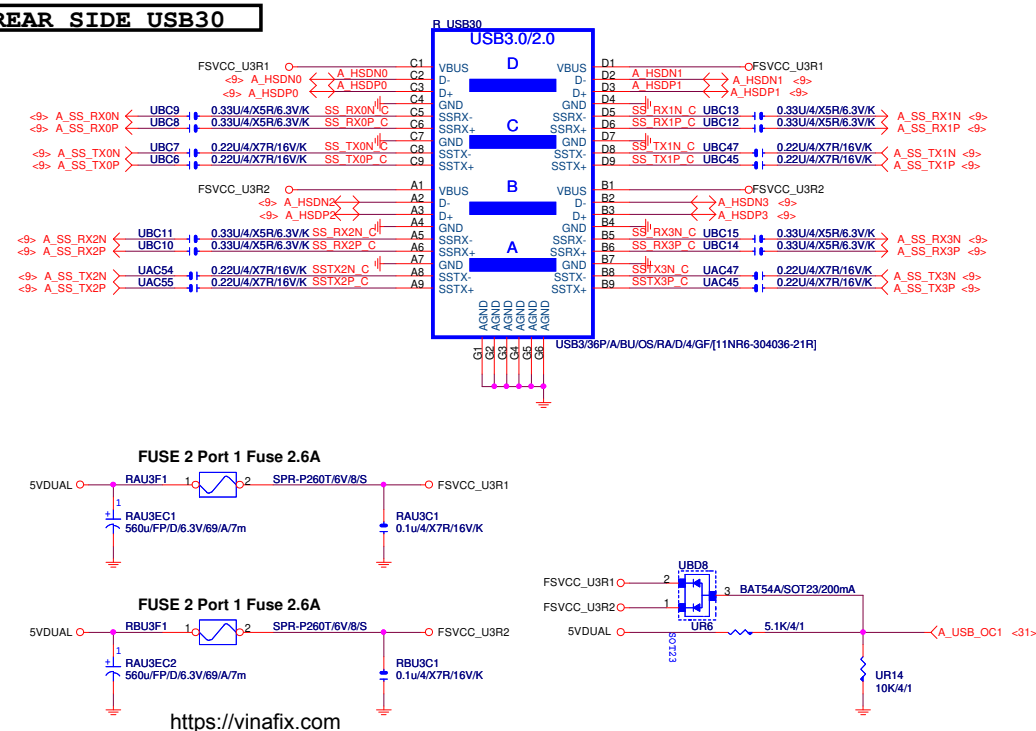
**FRONT SIDE USB2**

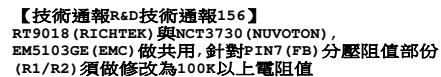
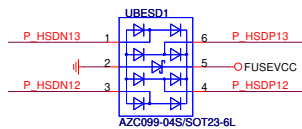
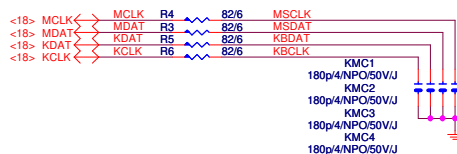


**FRONT SIDE USB1**



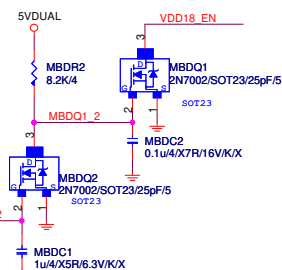
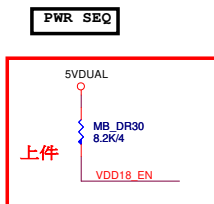
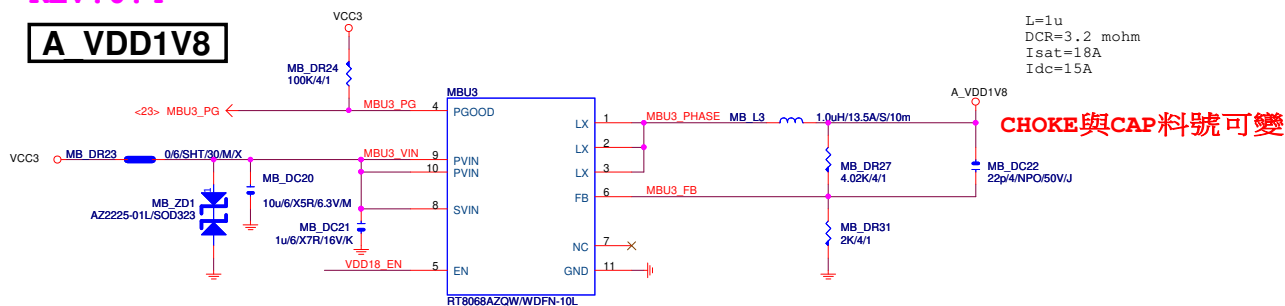
## REAR SIDE USB30





CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

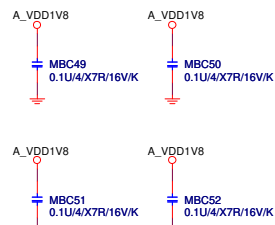
**A VDD1V8**



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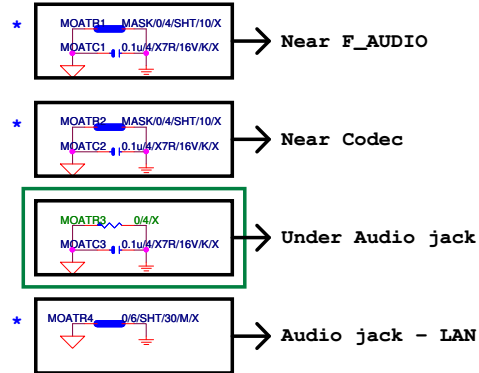
VPP CAP

\* 大電容 x0

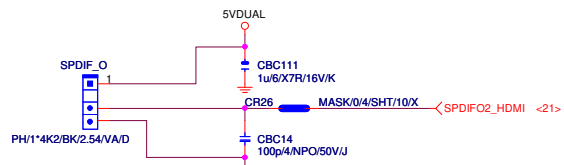


22u/6/X5R/6.3V/M  
**22u\*1PCS**



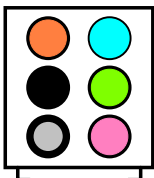


\*量産前,MOATR1/MOATR2/MOATR4 ....0ohm改short pad



For HDMI SPDIF (依SPEC保留或移除)

## AZALIA JACK

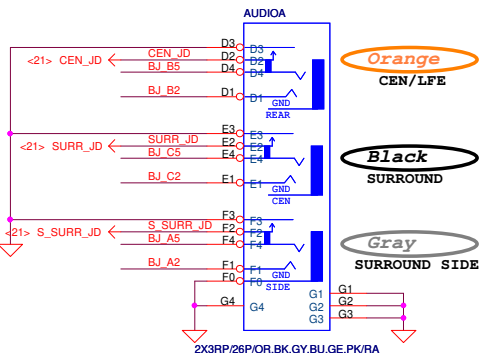
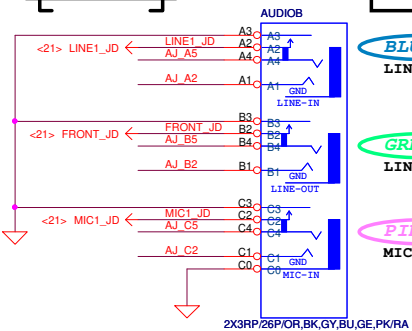


## AZALIA JACK

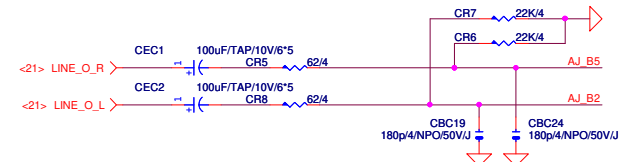
BLUE  
LINE-IN

GREEN  
LINE-OUT

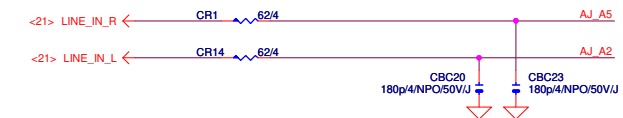
PINK  
MIC-IN



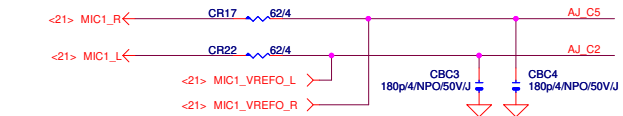
## LINE-OUT



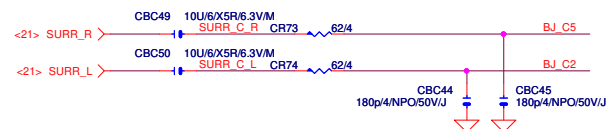
## LINE-IN



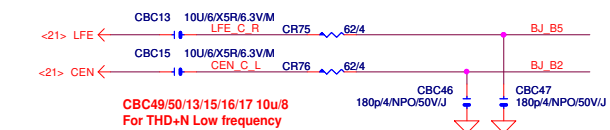
## MIC-IN



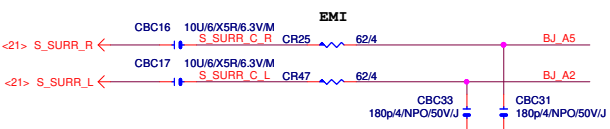
## SURROUND



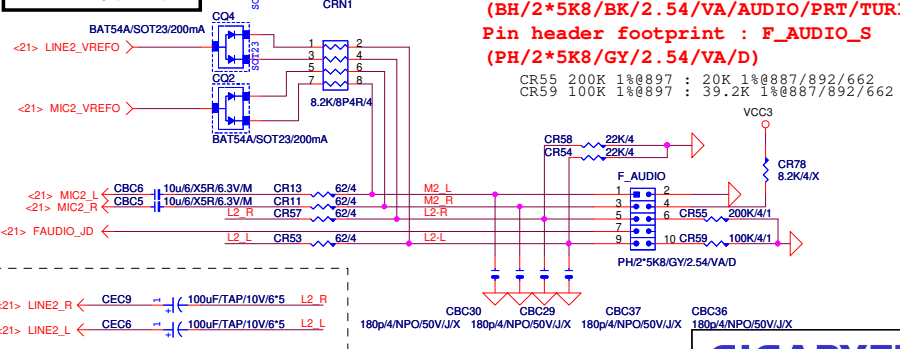
## CEN/LFE



## SURR BACK



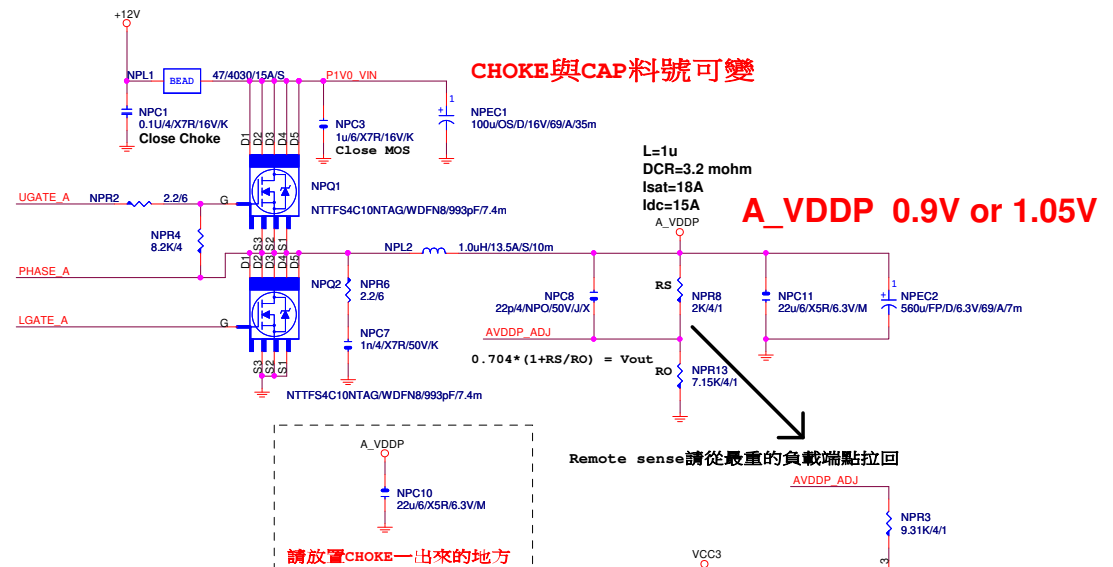
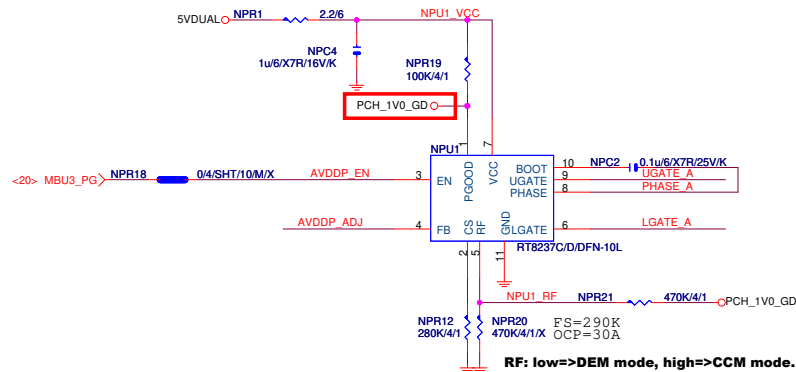
## AZALIA FRONT PANEL



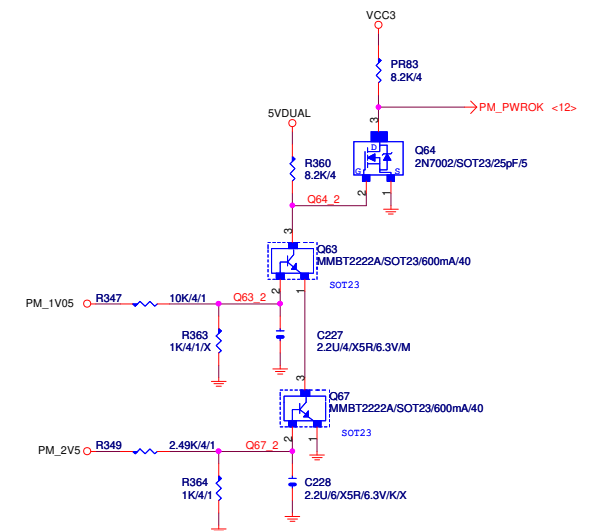
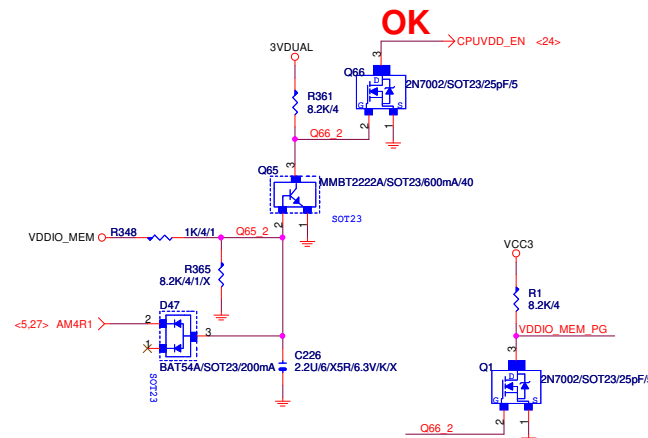
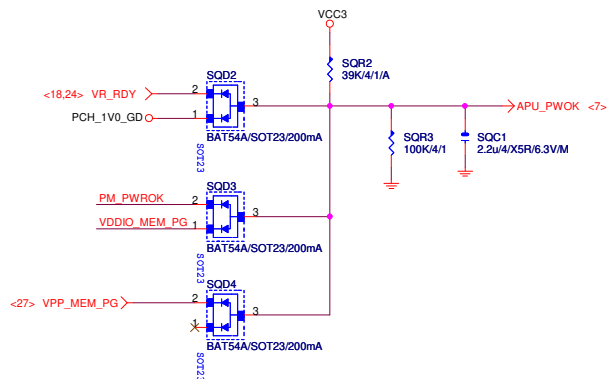
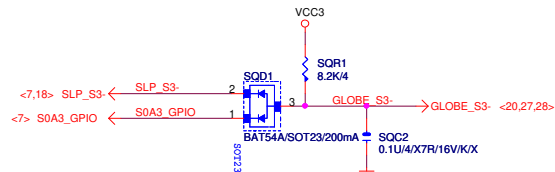
Box header footprint : F\_AUDIO  
(BH/2\*5K8/BK/2.54/VA/AUDIO/PRT/TUR180)  
Pin header footprint : F\_AUDIO\_S  
(PH/2\*5K8/GY/2.54/VA/D)

**GIGABYTE**™

Title			
AUDIO JACK			
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CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

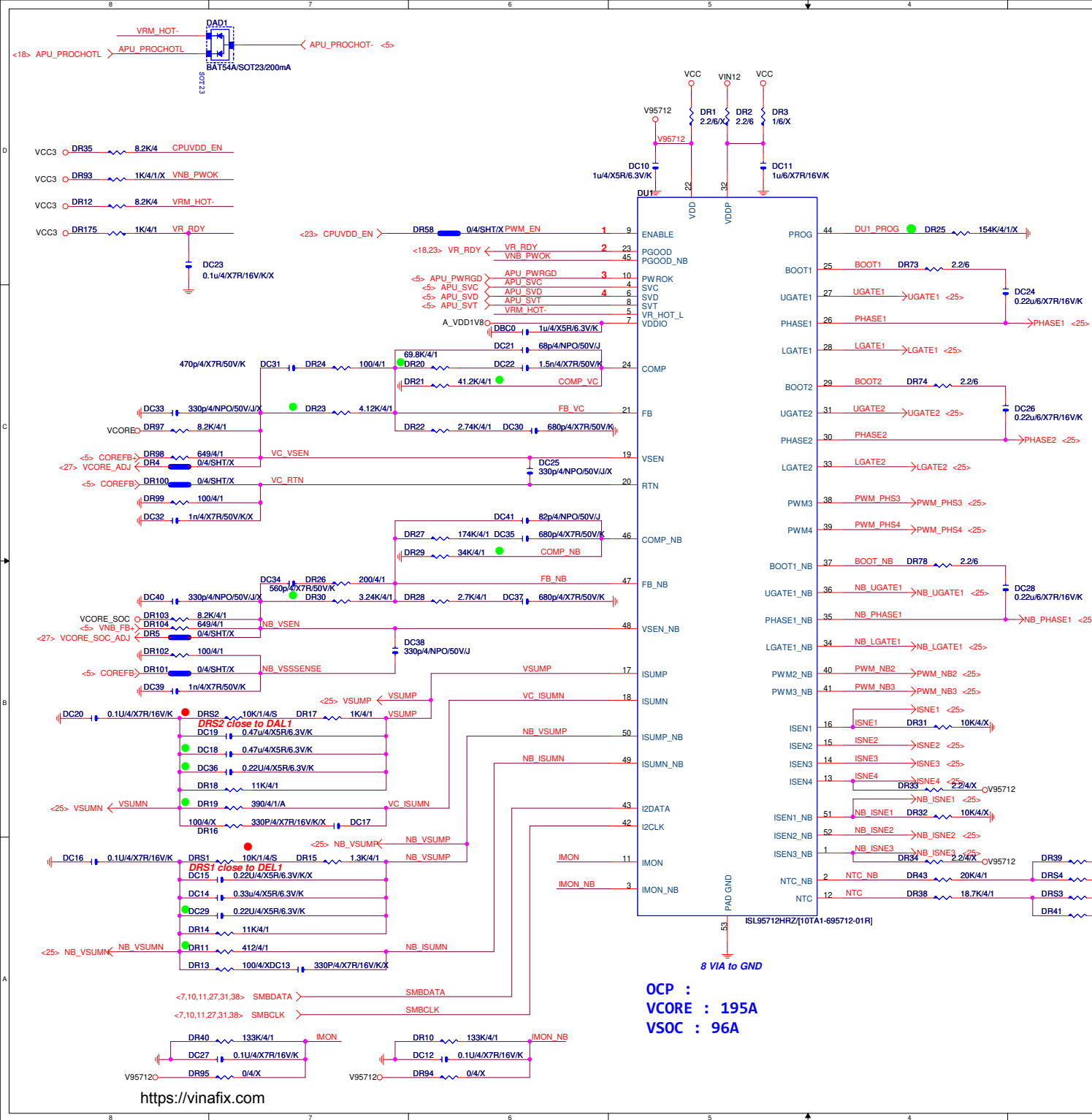


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## POWER SEQUENCE

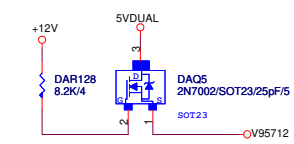
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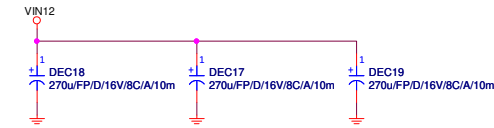


# 1.新增DAR128.DAQ5 (12V負壓線路)

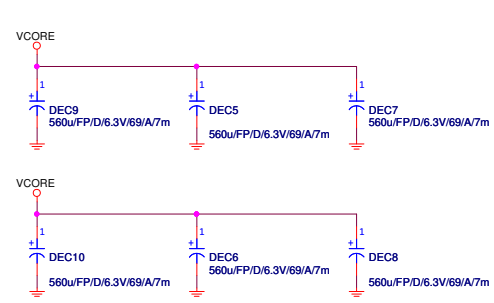
## 2.DR1改不上件



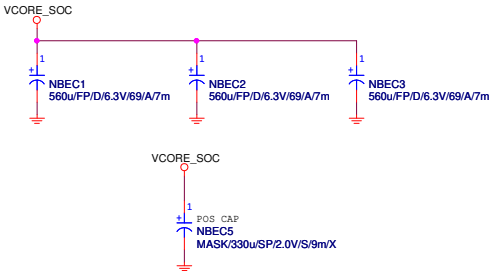
### VIN \* 3PCS



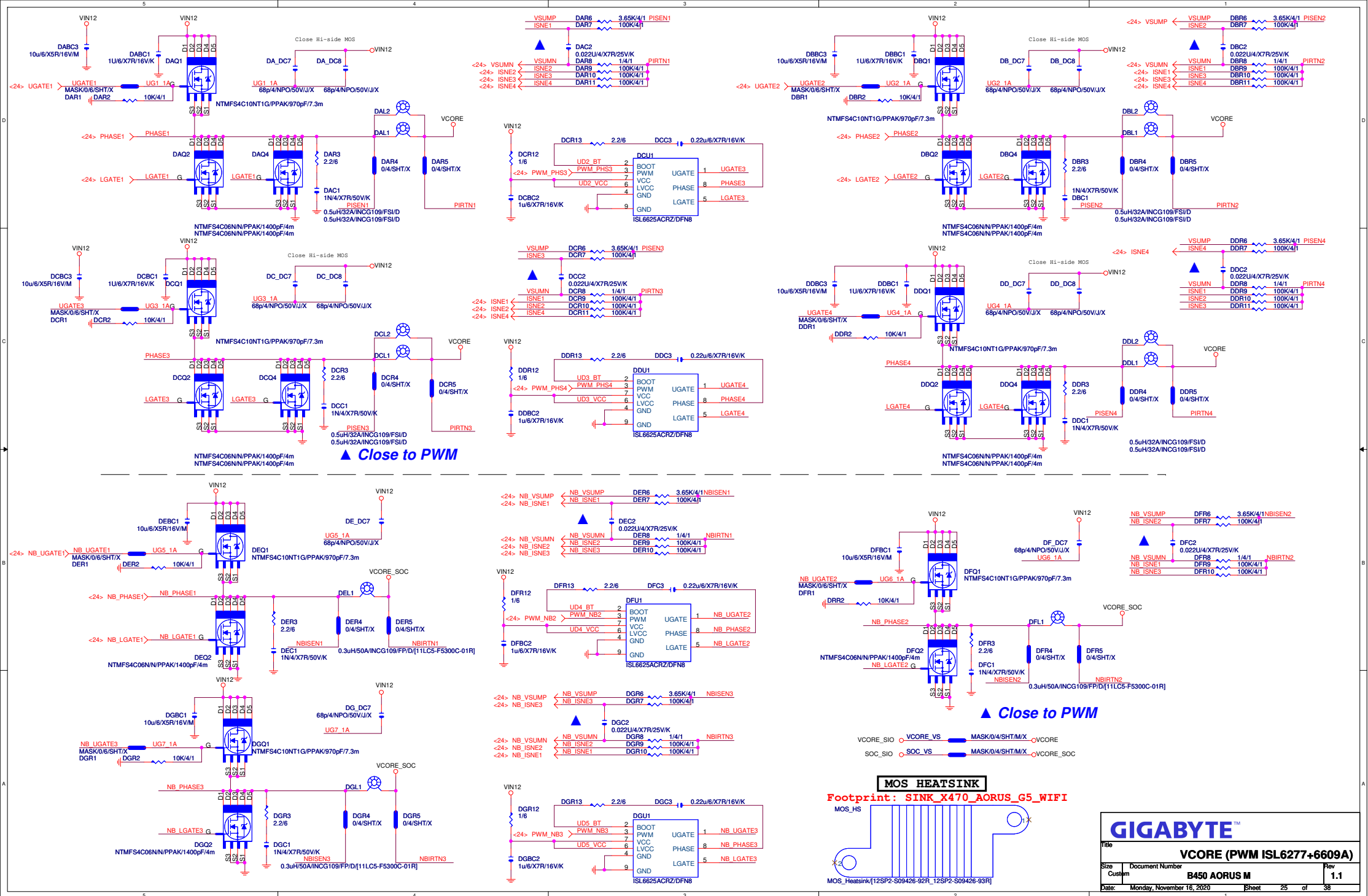
### VCORE \* 6 PCS

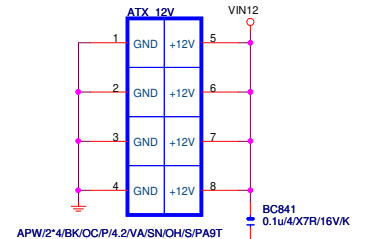
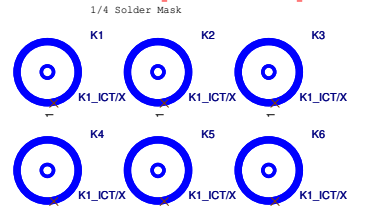
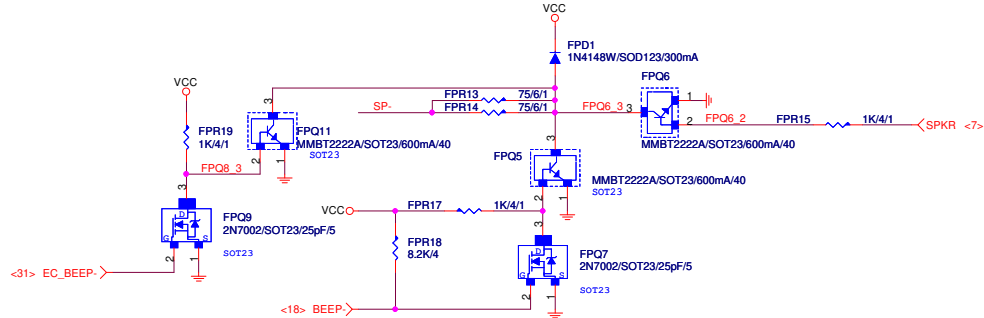
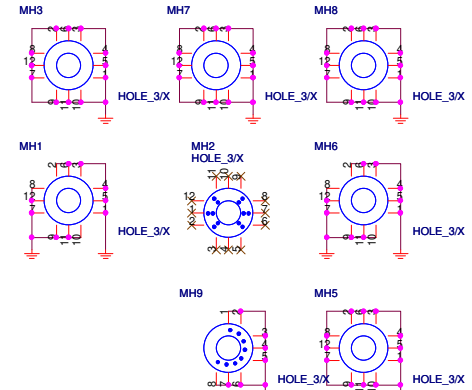
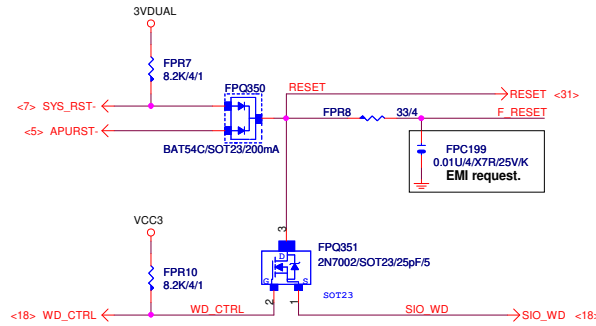
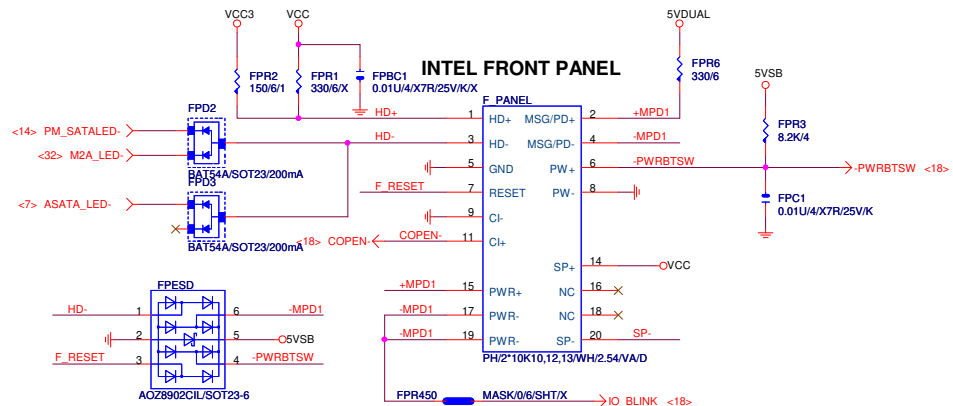


### VSOC \* 4 PCS



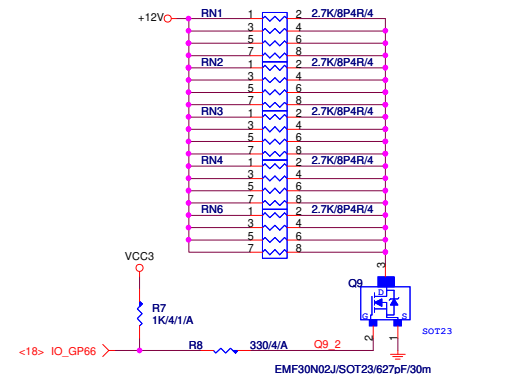
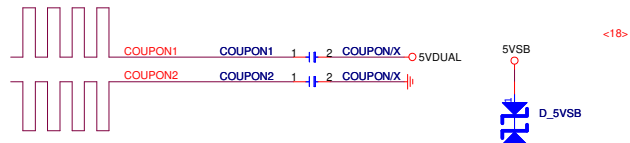
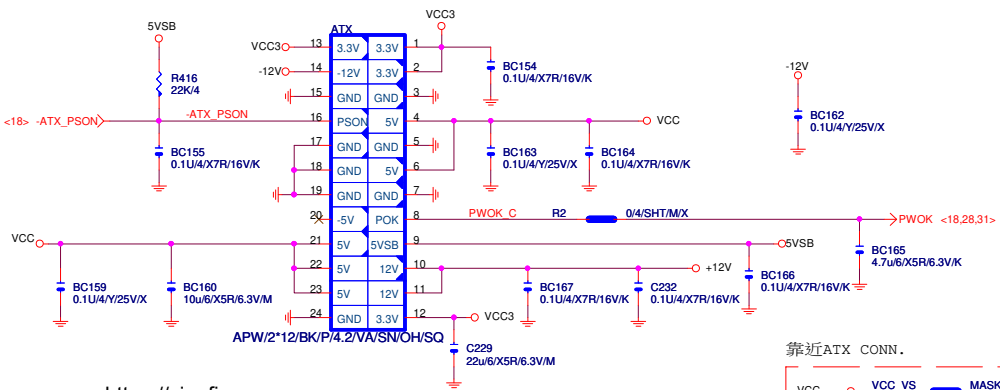






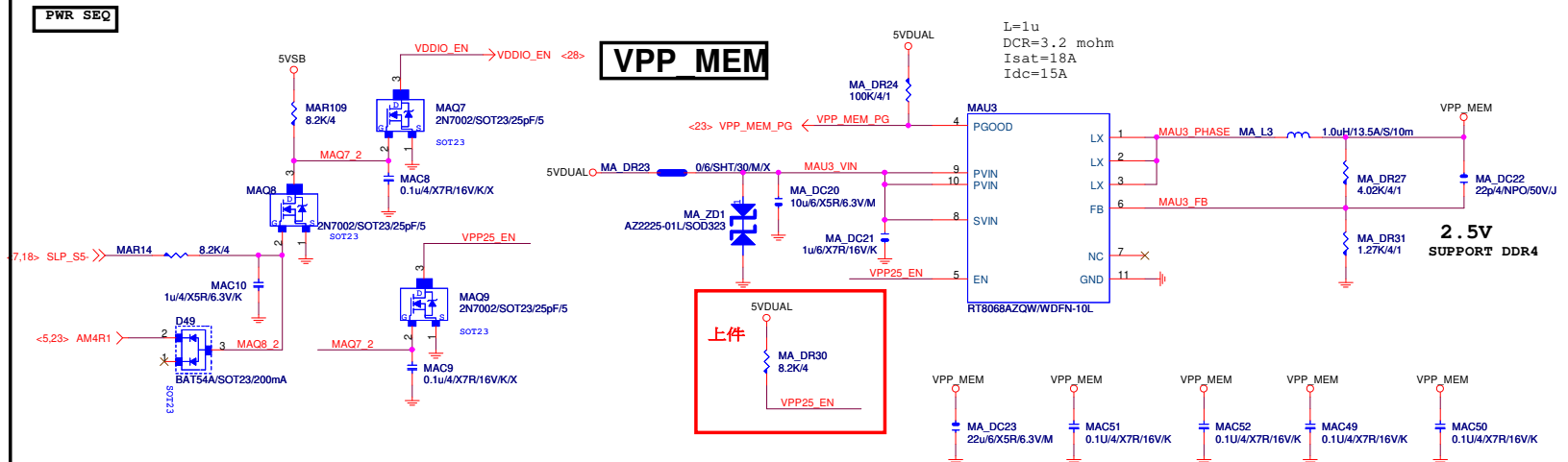
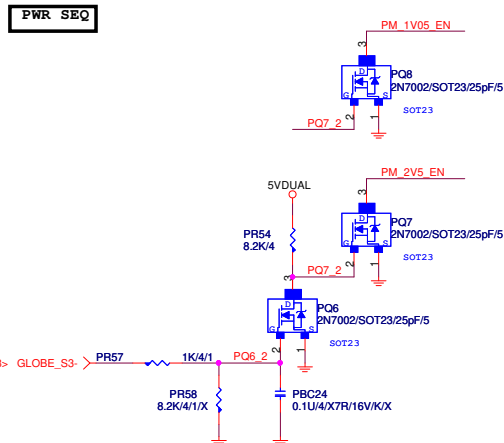
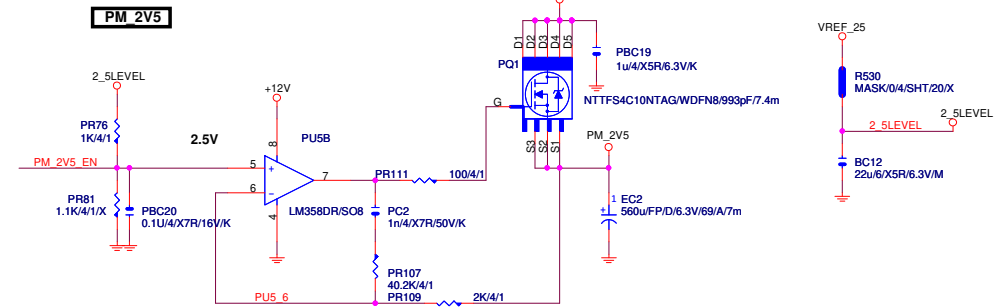
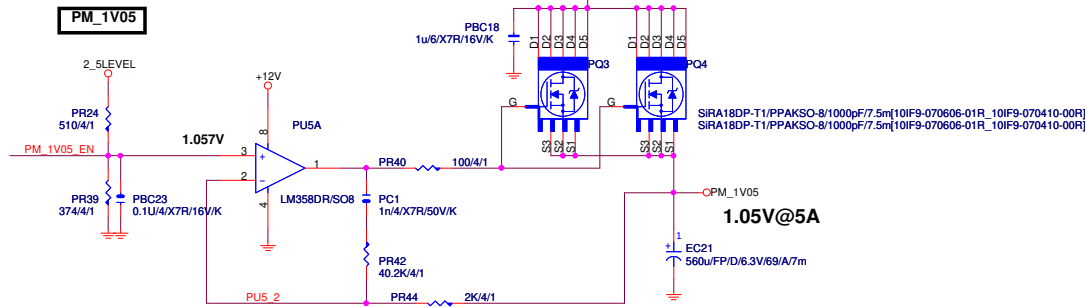
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### ATX POWER CONNECTOR

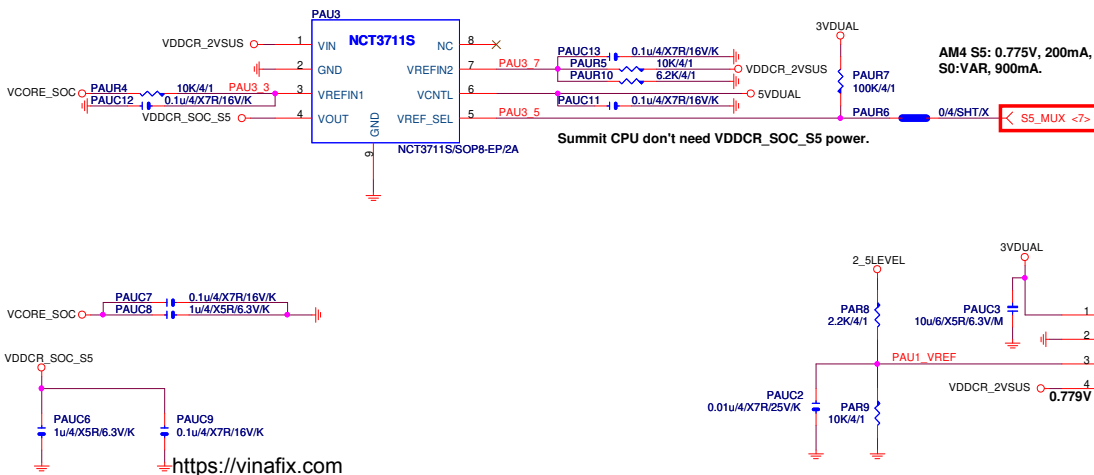


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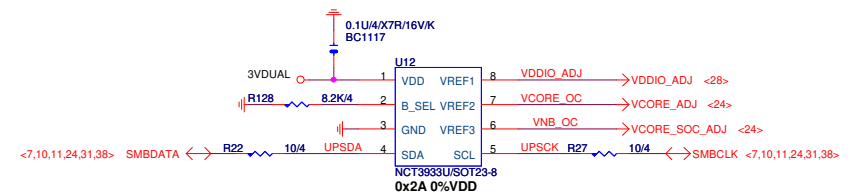
https://vinafix.com



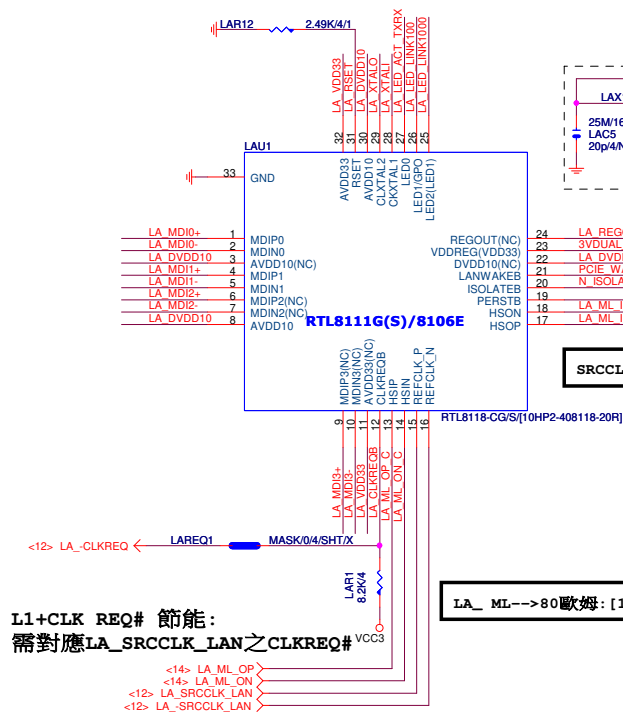
## VDDCR SOC S5



S5\_MUX: S0-->High, S5-->Low  
H: VDDCR\_SOC\_S5 will track VCORE\_SOC.  
L: If VCORE\_SOC < 0.775V (OR 0.85V), VDDCR\_SOC\_S5=0.775V.  
If VCORE\_SOC >= 0.775V (OR 0.85V), VDDCR\_SOC\_S5 will trace VCORE\_SOC.



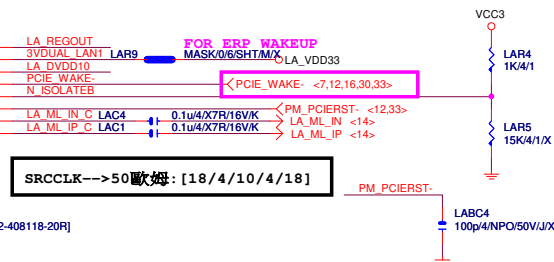




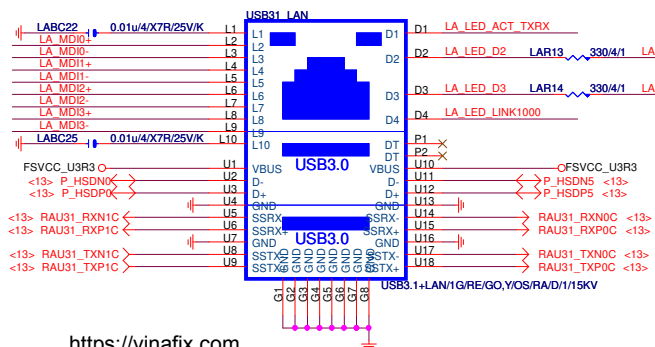
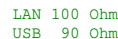
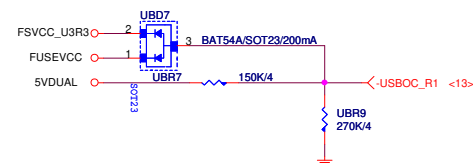
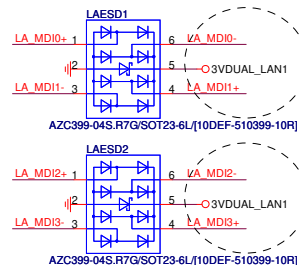
```

<14> LA_ML_OP
<14> LA_ML_ON
<12> LA_SRCCLK_LAN
<12> LA_SRCCLK_LAN

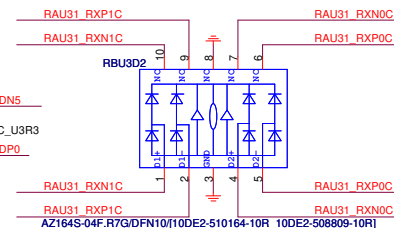
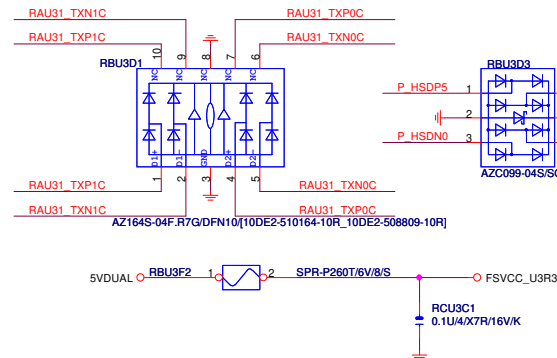
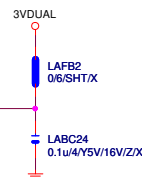
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MDI ESD

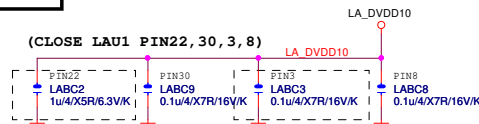


<https://vinafix.com>

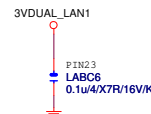


Title	RTL8111G , USB31
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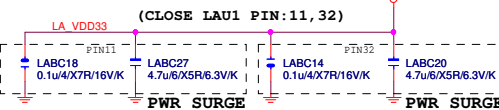
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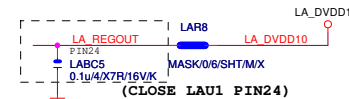
LABC2:1U CLOSE PIN22[REALTEK REQ]



(CLOSE LAU1 PIN23)

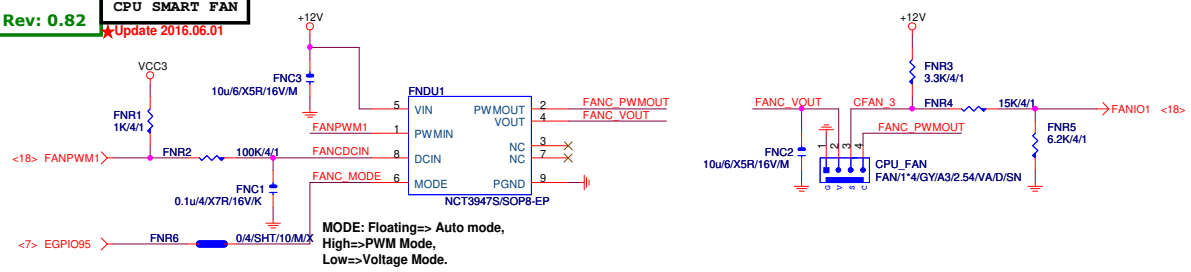


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LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]
```

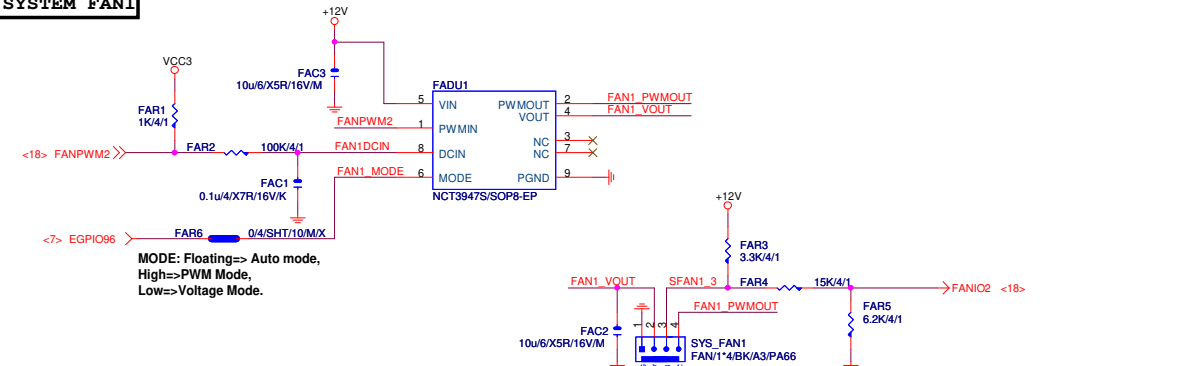


可變 3VDUAL\_LAN1 ○ LAPW1 MASK/0/4/SHT/M/X 3VDUAL \*

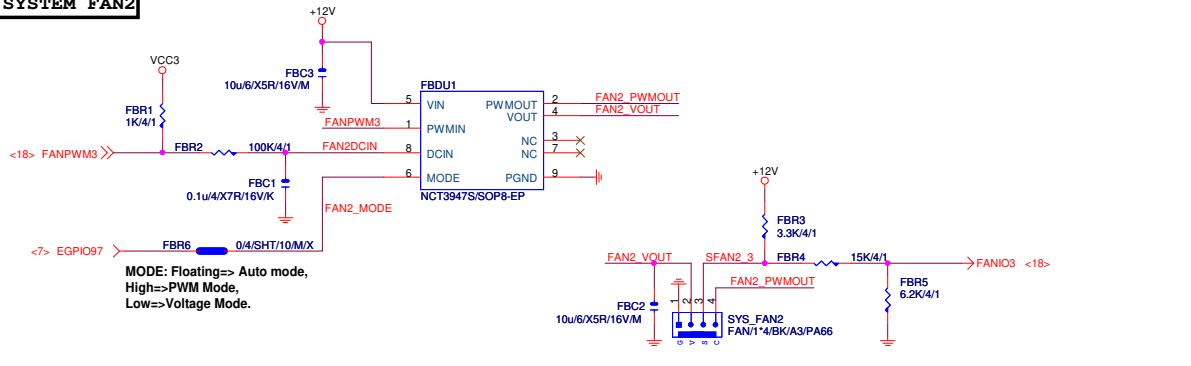
R2.0



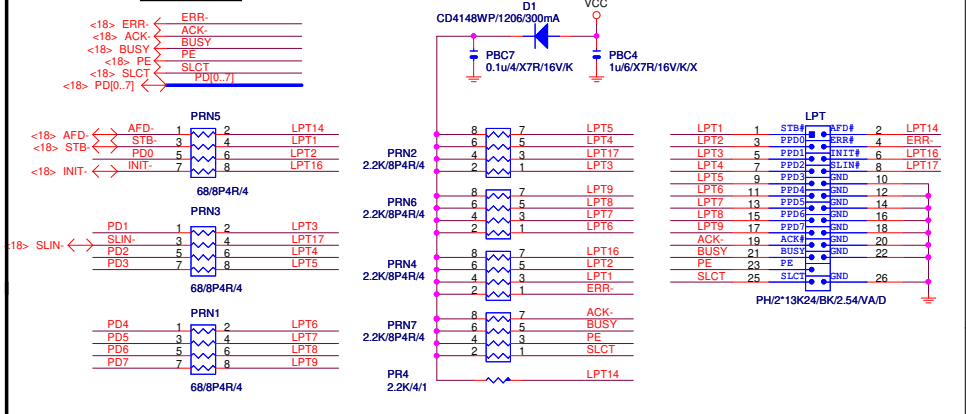
SYSTEM FAN1



SYSTEM FAN2

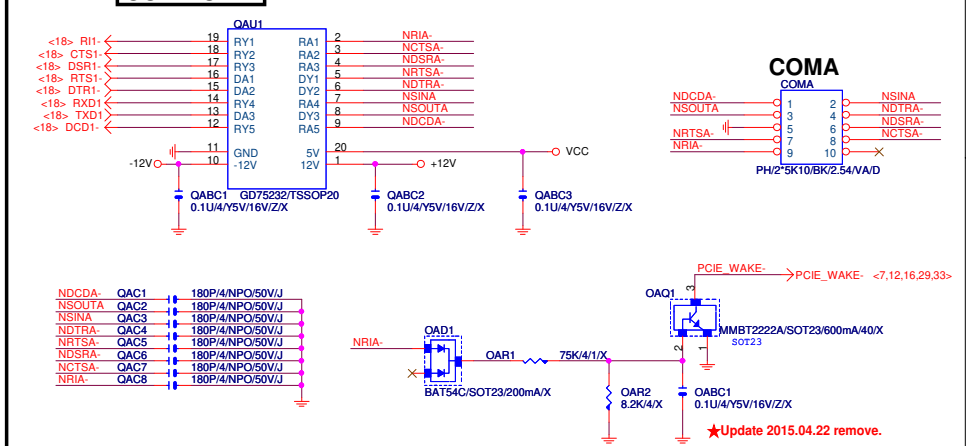


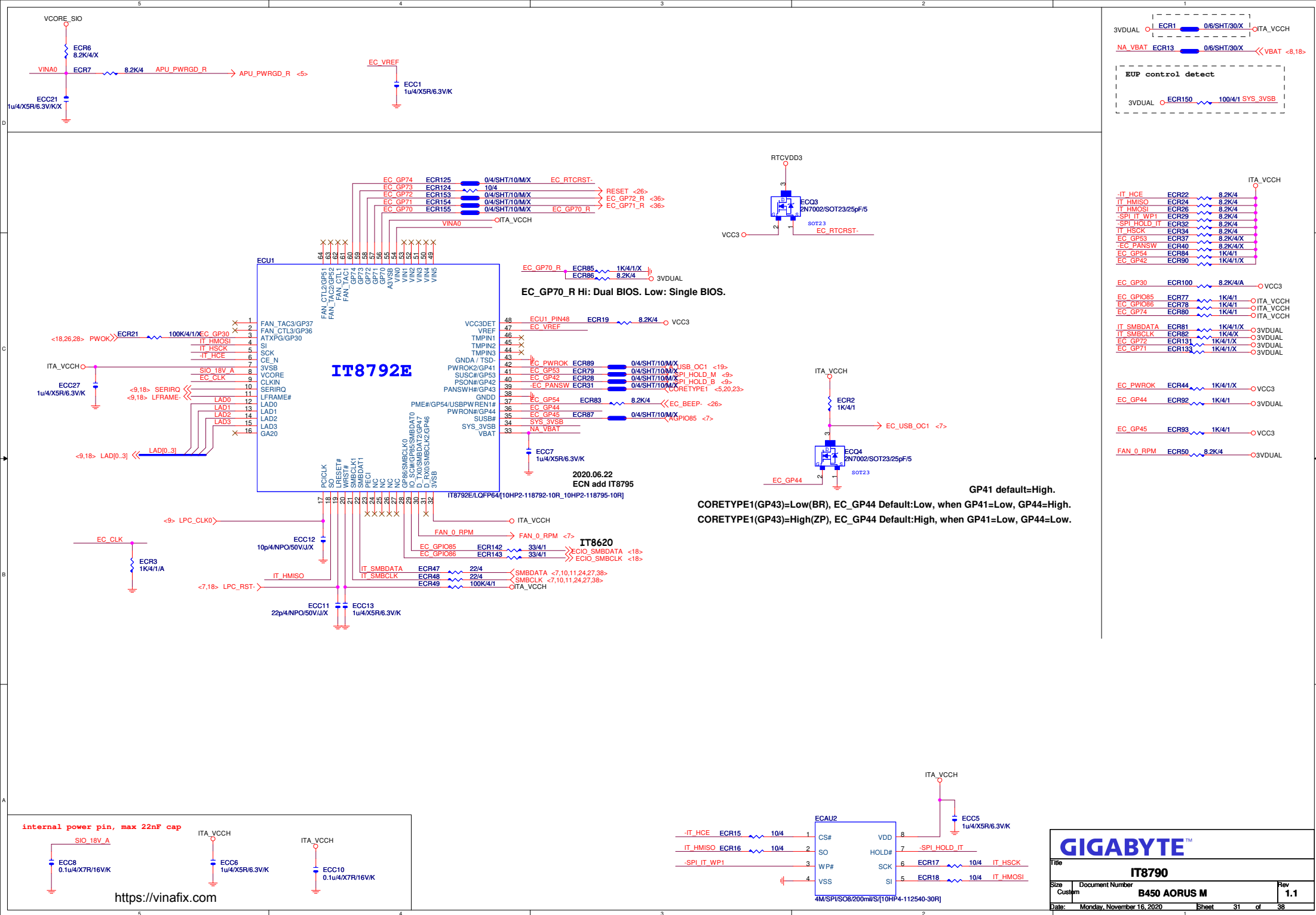
LPT PORT



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COM PORT





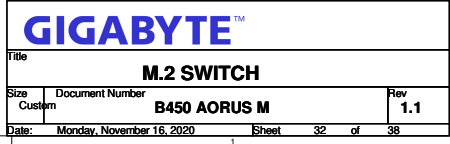
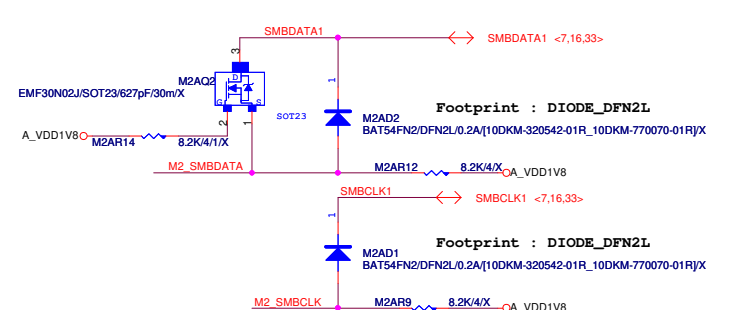
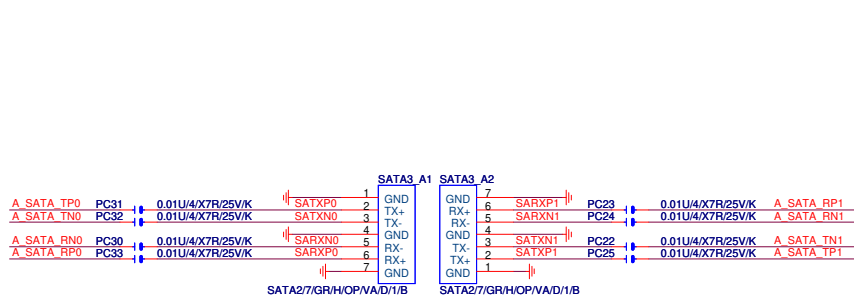
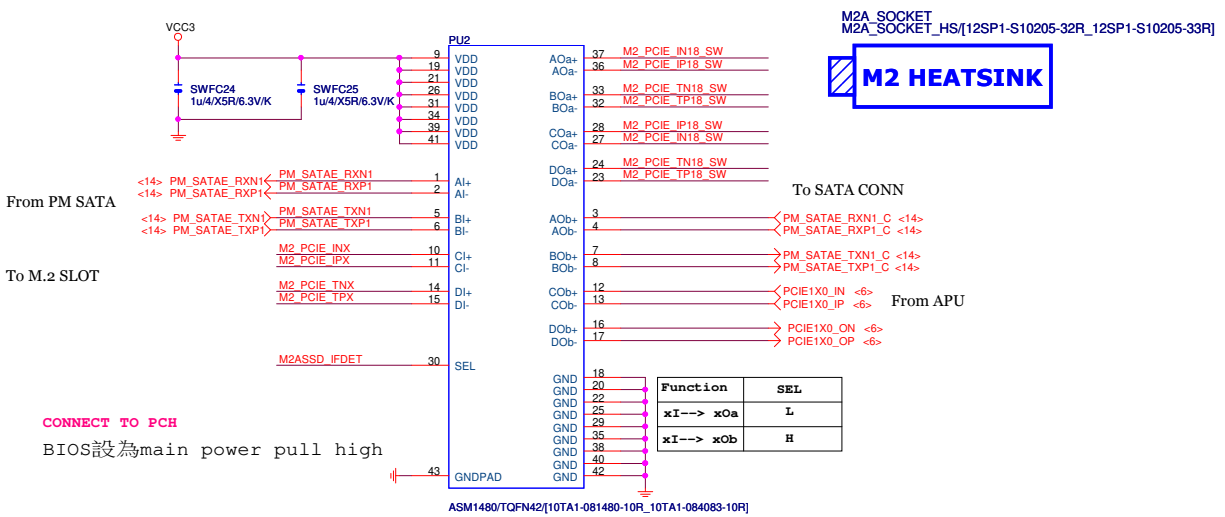
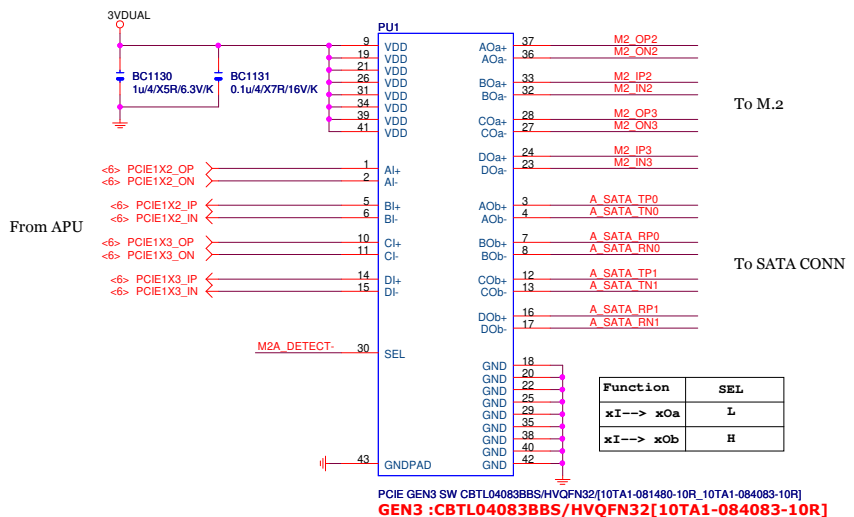
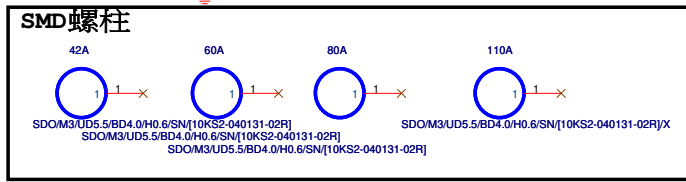
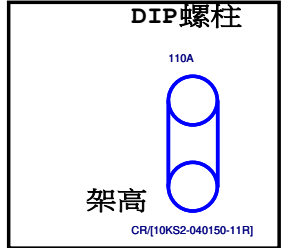
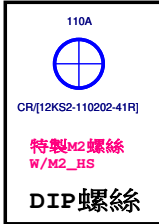
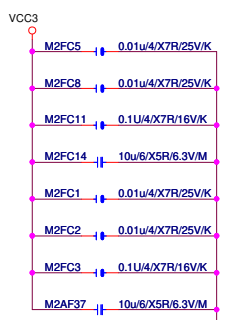
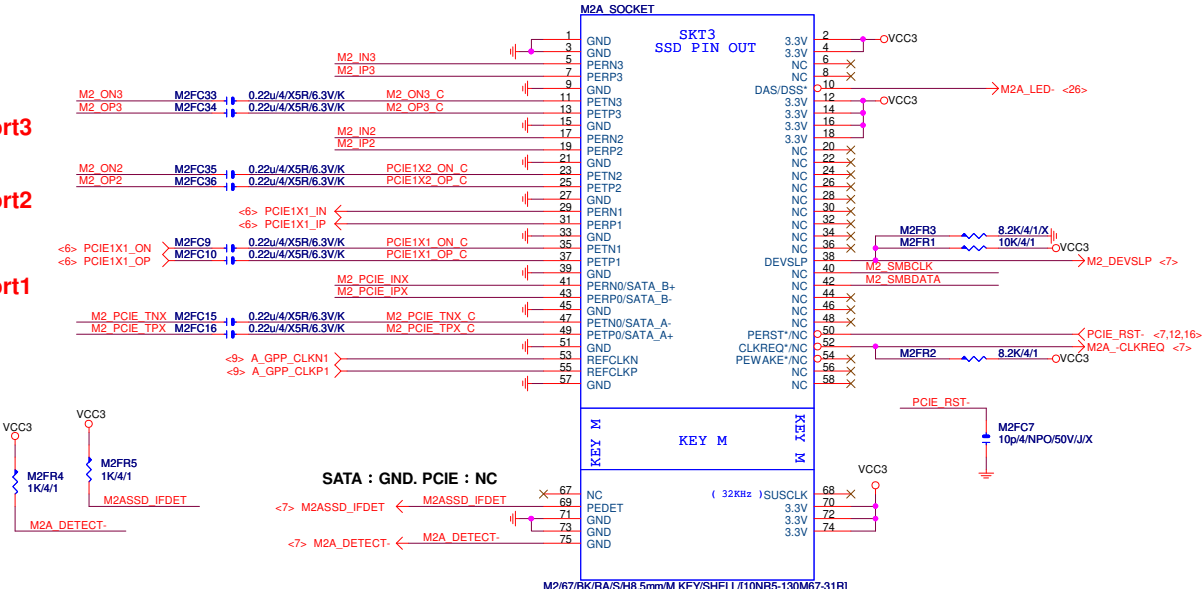
Rev 0.5

### M.2 Lane4 from AM4 port3

## M.2 Lane4 from AM4 port2

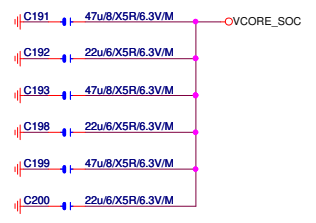
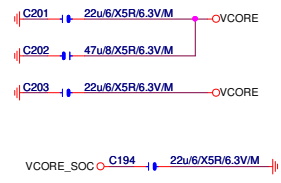
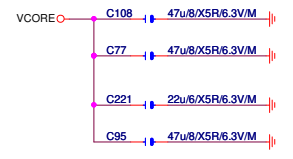
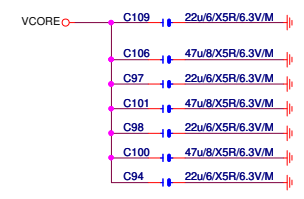
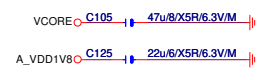
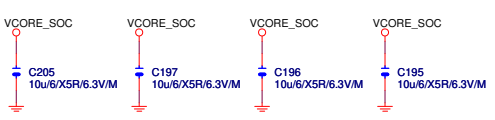
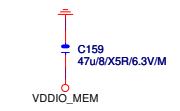
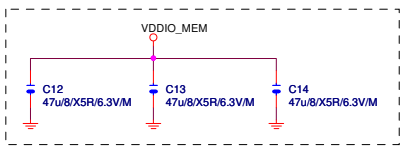
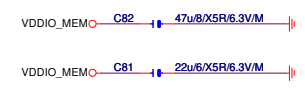
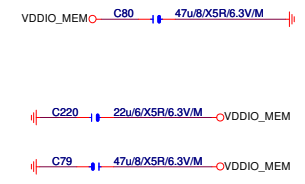
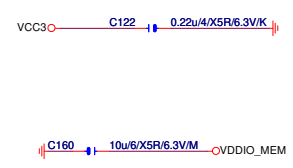
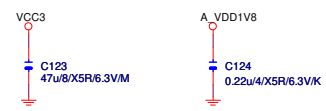
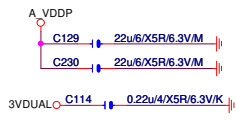
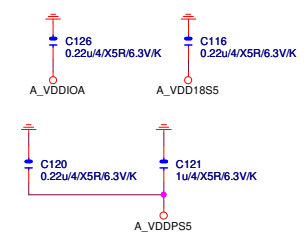
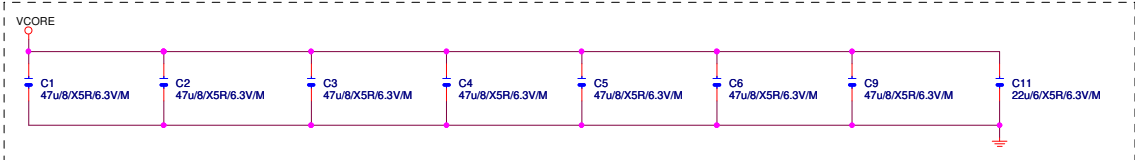
## M.2 Lane4 from AM4 port1

## by SWITCH Select





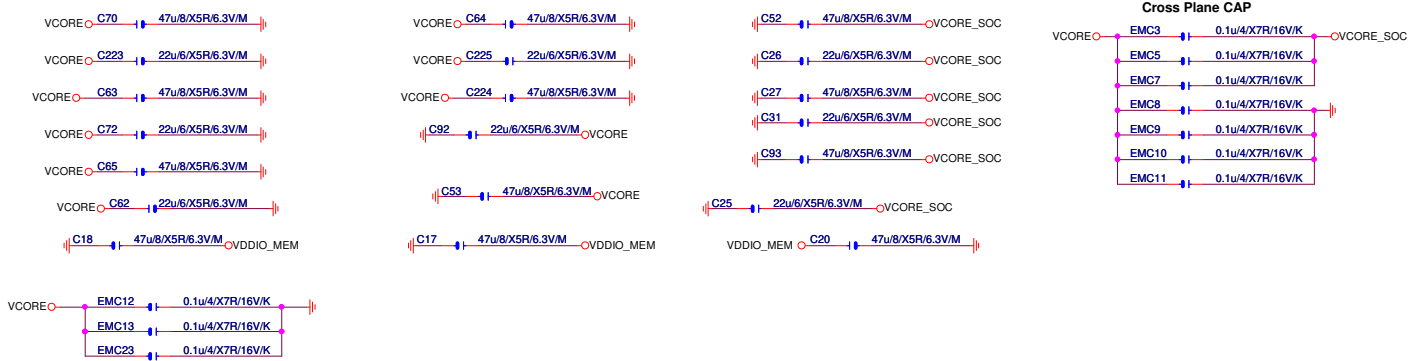




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<b>GIGABYTE™</b>			
<b>CPU BOTTOM</b>			
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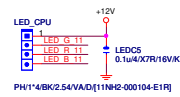
CPU TOP CAVITY



## 第一區 LED

FOR CPU 正發光 LED\*4  
(在CPU CHOKE之間,MOS\_HS下方,不外露)

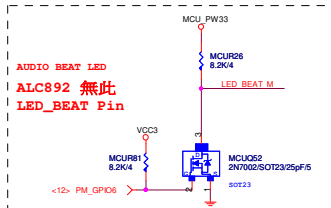
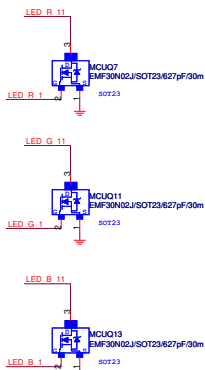
## AMD CPU\_FAN LED connector



## 第二區 LED

FOR DIMM 側發光 LED\*12  
(位置在DIMM兩側)

## 第一區 LED CONTROL



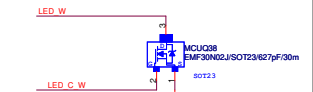
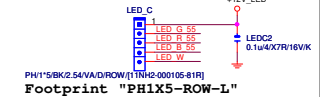
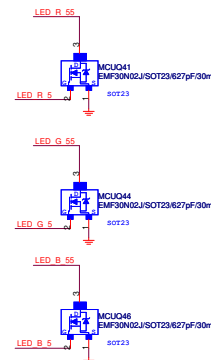
AUDIO BEAT LED  
ALC892 無此  
LED\_BEAT Pin

<12> PM\_GP06

## 第五區 LED

燈條 LED (LED\_C1放在PCB左邊板邊位置)

## 第五區 LED CONTROL



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LED\_C1 WHITE LED ON/OFF  
第五區 LED (外部燈條LED\_C1/LED\_C2)

第四區 LED (PCIE)

第三區 LED (DDR)

第二區 LED (CPU)

第一區 LED (CPU)

DEMO MODE Detect

AUDIO BEAT LED

DEMO MODE

DEMO MODE

DEMO MODE

DEMO MODE

DEMO MODE

DEMO MODE

DEMO MODE

DEMO MODE

DEMO MODE

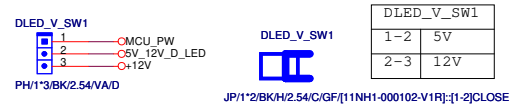
DEMO MODE

DEMO MODE

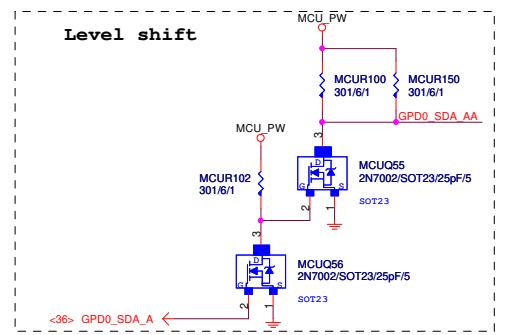
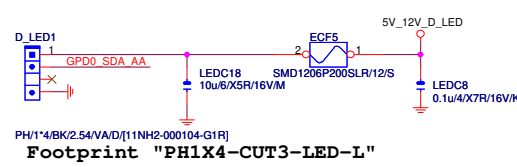
<https://vinafix.com>

Address:011

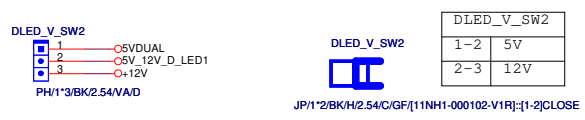
### 第六區 LED (靠近左上板邊位置)



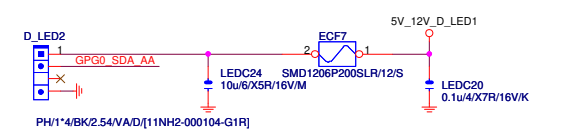
### Digital LED Strip1



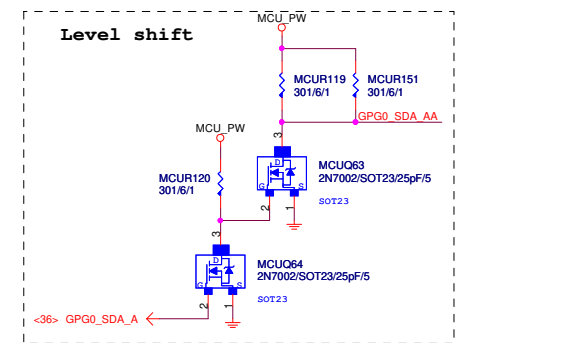
### 第七區 LED (靠近右下DDR板邊位置)



### Digital LED Strip2



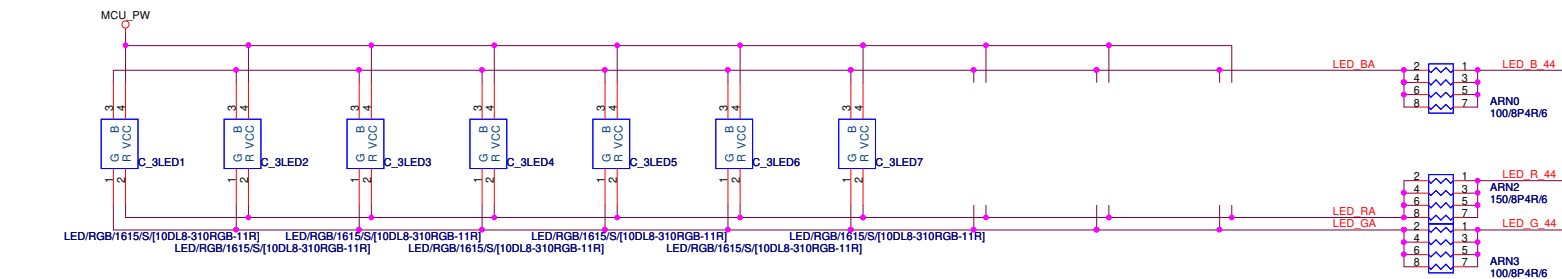
Footprint "PH1X4-CUT3-LED-L"  
(for pin-name 與 model-name 同方向)



第三區 LED

第四區 LED

FOR AUDIO 正發光 LED\*8 C\_3LED1~8)

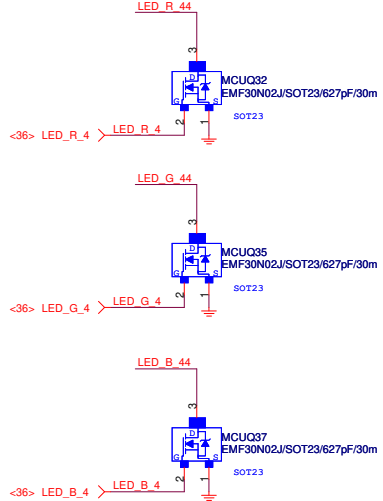


FOOTPRINT: LED-4P-RGB

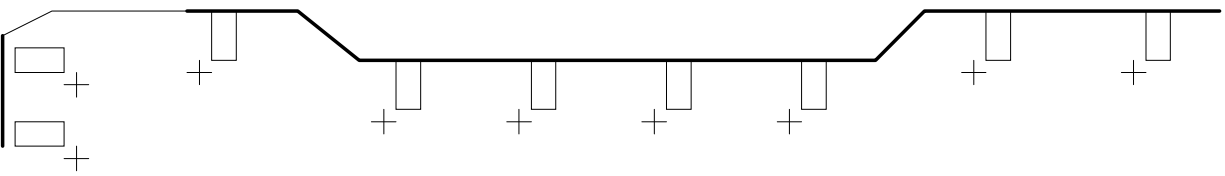
FOR PCIE16\_1 側發光 LED\*4  
(位置在PCIE16\_1 SLOT兩側各4顆)

FOR PCIE8 側發光 LED\*4  
(位置在PCIE8 SLOT兩側各4顆)

第四區 LED CONTROL



Audio Ground切割線+背面 RGB LED



RGB LED LAYOUT 注意事項 :

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下  
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU\_PW & MCU\_PW33電源一律走20mils
5. ECF1, ECF2, ECF3, ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils, 如: LED\_R\_1, LED\_G\_1, LED\_B\_1 .....
7. LED RGBW rule : W/S=10/5 mils 如: LED\_R\_11, LED\_G\_11, LED\_B\_11, LED\_W.....  
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils  
GPD0\_SDA\_B, GPD0\_SDA\_BB, GPD0\_SDA\_C, GPD0\_SDA\_CC

For AMD MCU update

